A Carbon Nanotube Neuron with Dendritic Computations

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***Abstract*—The design of a cortical neuron with carbon nanotube circuit elements that performs nonlinear dendritic computations is presented. The circuit design incorporates CNFETs, and was simulated using carbon nanotube spice models.**

I. Introduction

Neurons in the cortex are themselves complex systems, performing nonlinear dendritic computations. Furthermore, the scale of the cortex, with about 100 billion neurons, each with an average of 10^4 synapses [1] presents significant technological challenges. Nanotechnological solutions could allow the construction of a synthetic cortex containing trillions of synapses. One possible nanotechnology is carbon nanotubes that can behave as metallic wires as well as FETs. Our approach is to construct neural circuits that are biomimetic, that capture variations in neural behavior. We design such circuits in CMOS that can be fabricated, as well as in nanotechnologies for which SPICE models exist, and for which transistor behavior and the operation of simple circuits has been previously demonstrated.

We present the design of an electronic neuron with carbon nanotubes as circuit elements, and demonstrate the operation of this neuron with SPICE simulations. The synapse circuit has some capabilities to vary its behavior. The complexity of this particular neuron also lies in the variety of dendritic computations that can be implemented.

The biological synapse is itself complex, with controllable transmitters that can decrease or increase the excitability of the postsynaptic receptors. The activation probability of a given synaptic junction is regulated by the amount and timing of presynaptic and postsynaptic activity. Neurotransmitters must be present in sufficient amounts to develop post-synaptic potentials (PSPs), and the concentration of transmitters released can affect the height and duration of the PSP [1]. Action potentials impinging on the synapses could result in temporal summation of the resulting PSPs, increasing the likelihood of the post-synaptic neuron eventually firing.

Post-synaptic potentials on the dendritic arbor combine in complex ways [2]. These computations include linear, sublinear and superlinear additions of excitatory postsynaptic potentials (EPSPs), depending on the relative locations of the synapses. These dendritic computations affect the probability and frequency of neural firing.

Carbon nanotubes may support the scale of a synthetic cortex, being extremely small (a few nm. in diameter). Current flow is largely ballistic (comparable to the flow of electrons in free space), capacitances are in attofarads, and rise and fall times in picoseconds. Channel resistance is primarily due to the quantum resistance at the junction between the nanotubes and metallic connections, related to the differences in electron energy levels. This creates a challenge for neural circuit design since resistance cannot be adjusted easily. Current flow between drain and source is typically increased by using parallel nanotubes, although small adjustments can be made by varying nanotube diameter. Appropriate interfaces could be used to convert to biological signal levels and delays. Finally, nanotubes have been shown to induce minimum immune system reactions in living tissue, making carbon nanotube prosthetic devices desirable [3].

SPICE simulations have shown lower gate delay and energy per cycle for a carbon nanotube inverter over a 32nm CMOS inverter [4]. Furthermore, Paul *et al.* [5] demonstrated that carbon nanotube field-effect transistors (CNFETs) are less sensitive to the geometry-related process variations that are the major limitation on the performance of silicon MOSFETs. While it is difficult to precisely position CNTs on the substrate, Patil *et al.* have recently proposed a technique to design misaligned and mispositioned CNT immune circuits that can guarantee the correct function being implemented [6].

Single-walled carbon nanotubes avoid most of the fundamental scaling limitations of silicon [7]. Liu, Han and Zhou have demonstrated directional growth of high-density single-walled carbon nanotubes on a- and r-plane sapphire substrates [8]. This technique may enable registration-free fabrication of nanotube devices and lead to integrable and scalable systems, including synthetic cortex circuits. They have developed a novel nanotube-on-insulator (NOI) approach, and a way to transfer these nanotube arrays to flexible substrates.

Efforts have been made in recent years on modeling CNFETs (e.g. [9]) and CNT interconnects [10]. To evaluate CNFET circuit performance, a CNFET device model with a more complete circuit-compatible structure and including the typical device non-idealities was constructed [4]. That research presented a novel circuit-compatible compact SPICE model for short channel length (5nm 100nm), quasi-ballistic single wall

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carbon nanotube field-effect transistors (CNFETs).

We have designed and simulated a carbon nanotube neuron circuit that demonstrates dendritic computations. This neuron circuit contains synapses that capture the actions of neurotransmitters, ion channel mechanisms, and temporal summation of PSPs. We have focused on excitatory PSPs (EPSPs), and have chosen economy of size over exact waveforms, to facilitate scaling to cortical-sized biomimetic structures.

We have simulated a voltage adder with carbon nanotube circuit elements [11] to implement dendritic computations. This adder is tunable to support nonlinear summations of PSPs. We have designed a small dendritic arbor circuit, and shown how action potentials impinging on the presynaptic terminals of the arbor produce dendritic potentials that are a function of the EPSPs invoked at each synapse. We show that the electronic neuron fires when the cellular potential at the soma reaches a threshold value. We used the SPICE model in [4] to conduct all CNTFET simulations.

II. Background

Many electronic neurons have biomimetic features (e.g. [12]). The most notable research includes Mead's artificial retina [13], [14], followed by Boahen (e.g. [15] [16]) and more recently Hasler [17]. Hynna and Boahen report on a calcium spike circuit with replication of biological waveforms, and describe incorporation of the calcium spike circuit in an entire neuron circuit [18]. Liu and Frenzel's spike train neuron is a mixed-signal electronic model close to biological neurons, with a 10-transistor mixed-signal synapse [19]. An 8-transistor CMOS synapse [20] is close in scale and nature to our synapse, although they use the synapse for summation of inputs from many pre-synaptic sites. Analog synapses have been reported [21]. [22] and a phase-lock loop synapse has been reported [23]. Elias modeled dendritic computations as early as 1992 [24]. Hasler and Farquhar also model dendritic transmission [17], [12], as do others (e.g. Arthur [25] and Rasche [26]). Existing cable models could be integrated with our dendritic computations for a complete dendritic model. The strength of our model and similar models is the correspondence between individual circuit elements and specific physiological mechanisms in the biological neuron that allows us to vary neural behavior easily with control inputs. This, and our choice of carbon nanotube technology, differentiates our work.

III. The Carbon Nanotube Neuron Circuit

Our basic model for a cortical neuron, shown in Figure 1, consists of three types of sub-modules: the synapse [27], the dendritic arbor [27] and the axon hillock. The carbon nanotube synapse circuit, Figure 2, operates as follows: The simple action potential used here is an approximation of a typical biological action potential [28]. An incoming action potential will cause the potential in the synaptic cleft to rise, modeling the biological concentration of neurotransmitters released from the presynaptic neuron into the cleft, where they bind to receptor proteins on the recipient (postsynaptic)

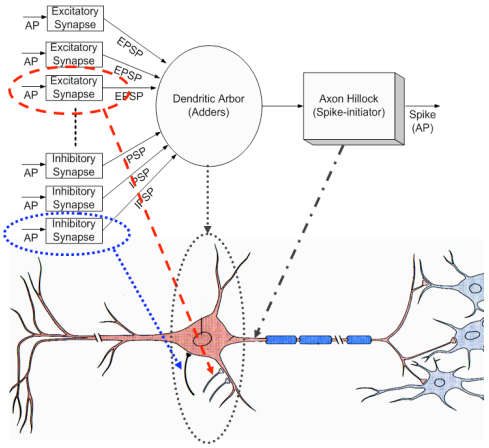

Fig. 1. A system block diagram of the cortical neuron model with a pyramidal neuron cartoon

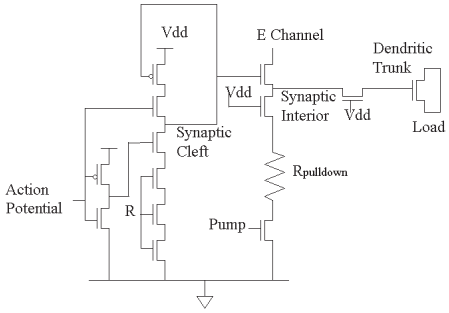

Fig. 2. The Carbon Nanotube Synaptic Circuit

neuron, causing the potential across the postsynaptic neural membrane to change.

Once the neurotransmitters have been released from the presynaptic terminal and bound in the postsynaptic terminal, they will be cleared for reuse by reuptake mechanisms modeled via the pull-down network attached to the synaptic cleft [1]. The re-uptake control voltage, R can be tuned.

The increase in potential in the synaptic cleft will temporarily cause the potential at Synaptic Interior to rise. This models the increased conductance of neurotransmitter-gated ion channels and the subsequent influx of charge carrying ions (e.g. sodium). A tunable pull-down network controls the cell interior's return to resting potential (steady state).

The synaptic interior potential is transferred through a resistive connection to the dendritic trunk, which carries the postsynaptic potential to the dendritic arbor.

The adder circuit [11] is shown in Figure 3. A block diagram of the dendritic arbor portion is shown in Figure 4. There are four synapses in the arbor, each on a separate dendritic branch. Our axon hillock circuit is shown in Figure 5. In a biological neuron,the axon hillock has the highest density of sodium channels, resulting in the lowest threshold (-55mV compared to elsewhere in the neuron) to initiate an action potential. If the summation of post-synaptic potentials (PSPs) reaches the

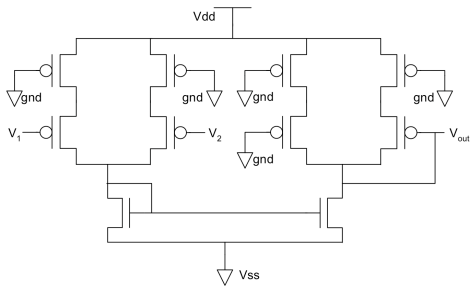

Fig. 3. The Voltage Adder

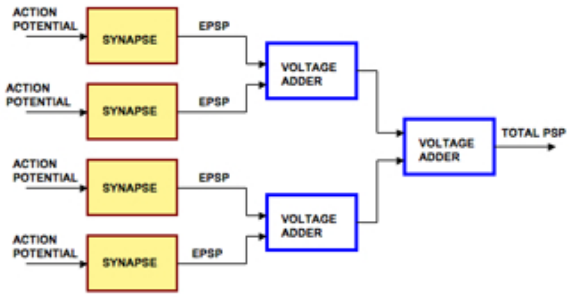

Fig. 4. The Dendritic Arbor Portion

threshold value, the axon hillock circuit will generate a spike. This circuit behaves in a similar fashion to a self-resetting CMOS circuit, receiving a rising edge and producing a pulse whose width is controlled by the gate delay of the inverter shown in Figure 5. To mimic a fast rising phase (due to the rapid increase of the sodium channel conductance) and a slower falling phase (due to the slow increase of the potassium channels' conductances) of an action potential, we adjusted the pull-up and pull-down strength of transistors X8 and X7. All the other transistors were tuned to model the time courses (time constants) in the dynamic machanisms of the voltage-gated ion channels.

In our archetypical biological neuron, potentials range from around -75mV to +40mV with action potentials peaking around +40mV. Since the carbon nanotube neuron is designed to operate with Vdd around 0.9V and with 0.0V (Ground) as the resting potential, the potentials were scaled accordingly, with 0V circuit potential corresponding to -75mV biological potential and 0.9V circuit potential corresponding to 40mV biological potential. Likewise, we scaled the delays with about 1 ms in the biological neuron scaling to about 10 ps in the nanotube neuron [28]. It should be noted that the fanin and fanout of cortical neurons are sufficient to significantly slow operation of artificial cortical neurons in practice.

IV. Experiments with the Dendritic Arbor Circuit

The postsynaptic potential appearing at the dendritic trunk is approximately 14% of the action potential and the duration is about 6 times as long as the action potential, similar to EPSPs described in the literature. We performed several experiments. We were able to tune the adders for linear

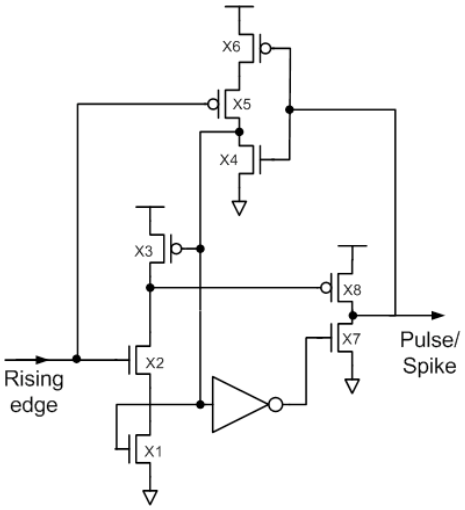

Fig. 5. Circuit diagram of the axon hillock module

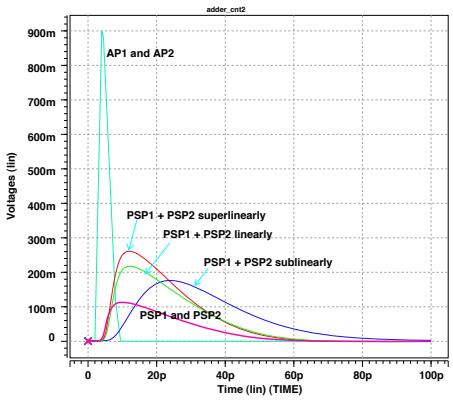

Fig. 6. EPSPs Summed Linearly, Sublinearly, and Superlinearly

summation. In a second experiment, we simulated two action potentials (APs) arriving at staggered times so that the two EPSPs peaked at different times, demonstrating temporal and spatial summation.

A third experiment shows the nonlinear PSP computations possible using our circuitry, in Figure 6. A final experiment illustrated the summation of weak and strong EPSPs.

V. Experiments with the Complete Cortical Neuron Model

The neuron was tested with action potentials input to each synapse, and the output of the neuron measured. The input action potential (the red trace) is applied to each synapse module and the generated action potential (the blue trace) is captured at the axon-hillock node in Figure 7. The dendritic arbor module was built with linear-summation mode adders. The sum of EPSPs (the dark grey trace) exceeded the threshold of the axon hillock therefore the neuron fired. When we input no action potential (eg. 0V) to some synapses, the summation of EPSPs is below the threshold to initiate a spike at the

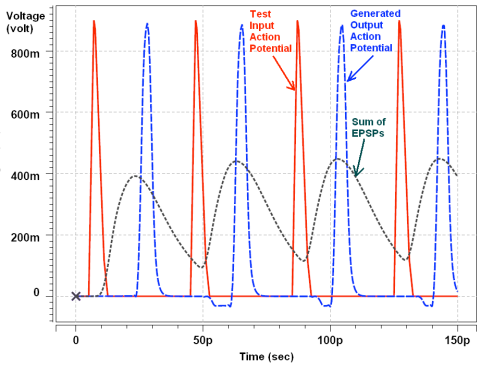

Fig. 7. Simulation result of the spiking neuron circuit with load synapse

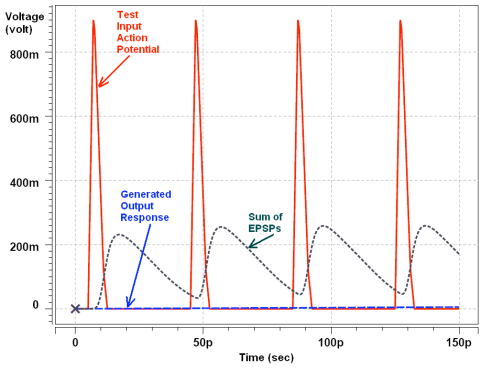

Fig. 8. Result of the spiking neuron circuit with insufficient dendritic potential

axon hillock. The blue trace in Figure 8 represents the non-spiking output of the axon hillock. The particular neuron we modeled in this paper fired only when a majority of EPSPs were presented. This reflected the circumstances where not enough PSPs have accumulated in the dendritic arbor of a biological neuron to cause it to fire.

Power consumption was compared to a similar CMOS neuron. The circuit consumed about 93% less power compared to CMOS (180nm technology.) According to International Technology Roadmap for Semiconductors (ITRS), while CMOS scaling will significantly reduce feature sizes by 2022, the power supply voltages will only decrease modestly, making carbon nanotube circuits a low-power alternative.

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