Alice Cline Parker

https://ceng.usc.edu/~parker/BioRC_research.html

Employment History

- **Emerita Professor, Dean's Professor, Professor**, Department of Electrical Engineering-Systems, University of Southern California, 9/91 to present, **Associate Professor**, 9/83 to 9/91, **Assistant Professor**, 9/80 to 9/83.

- **Vice Provost for Research and Graduate Studies**, University of Southern California, 1/96 to 8/97.

- **Vice Provost for Research and Dean of Graduate Studies**, University of Southern California, 7/94 to 12/95.

- **Division Director**, Computer Engineering, Department of Electrical Engineering-Systems, University of Southern California, 9/91 to 1/94, **Group Leader**, Computer Engineering, 1983-84.

- **Assistant Professor**, Department of Electrical Engineering, Carnegie-Mellon University, 1/75 to 8/80.

Education

- **Ph.D.** (Electrical Engineering), North Carolina State University, 1975.

- **M.S.** (Electrical Engineering), Stanford University, 1971.

- **B.S.** (Electrical Engineering), North Carolina State University, 1970.

SELECTED HONORS AND AWARDS

* 2022 IEEE-USA Award for Distinguished Literary Contributions Furthering Public Understanding and the Advancement of the Engineering Profession "For inspiring the next generation of women in engineering through the book "Women in Microelectronics."

*Engineer's Council Distinguished Engineering Educator Award 2021

* WiSE Architects of Enduring Change Award 2020

*Orange County Engineers Council Distinguished Engineer Award 2018

Dean's Professor of Electrical Engineering 2017-2023

*NCSU ECE Hall of Fame Award 2017

**Life Fellow of the IEEE*
** IEEE Golden Core Award*
* ASEE Sharon Keillor Award for Women Engineers, 2009

* Service Award, South Central Scholars, 2008
* Outstanding Teaching Award, Viterbi School of Engineering, USC 2006
* NSF Award for Women Scientists and Engineers 1990
* ACM Service Award 1988
* ACM Distinguished Lecturer
* National Science Foundation Fellow 1970

PUBLICATIONS

Journal Articles

1. **"Biological Underpinnings for Lifelong Learning Machines,"** Dhireesha Kudithipudi[1,*], Mario Aguilar-Simon[2], Jonathan Babb[3], Maxim Bazhenov[4], Douglas Blackiston[5], Josh Bongard[6], Andrew P. Brna[2], Suraj Chakravarthi Raja[7], Nick Cheney[6], Jeff Clune[8], Anurag Daram[1], Stefano Fusi[9], Peter Helfer[1], Leslie Kay[10], Nicholas Ketz[11], Zsolt Kira[12], Soheil Kolouri[11], Jeffrey L. Krichmar[13], Sam Kriegman[24], Michael Levin[5], Sandeep Madireddy[14], Santosh Manicka[5], Ali Marjaninejad[7], Bruce McNaughton[13], Risto Miikkulainen[15], Zaneta Navratilova[13], Tej Pandit[1], Alice Parker[7], Praveen K. Pilly[11], Sebastian Risi[16], Terrence J. Sejnowski[4,17], Andrea Soltoggio[18], Nicholas Soures[1,19], Andreas S. Tolias[20], Dar´ıo Urbina-Mele´ndez[7], Francisco J. Valero-Cuevas[7], Gido M. van de Ven[20], Joshua T. Vogelstein[21], Felix Wang[22], Ron Weiss[3], Angel Yanguas-Gil[14], Xinyun Zou[13], and Hava Siegelmann[23] , *Nature Machine Intelligence,* Feb. 2022 , *Nature Machine Intelligence,* Feb. 2022
2. "A Brain-plausible Neuromorphic On-the-fly Learning System Implemented with Magnetic Domain Wall Analog Memristors, " Kun Yue, Yizhou Liu, Roger K. Lake and Alice C. Parker, in *Science Advances*, April 26, 2019, Vol. 5, number 4, DOI: 10.1126/sciadv.aau8170.

3. "An Astrocyte Neuromorphic Circuit that Influences Neuronal Phase Synchrony," Yilda Irizarry-Valle and Alice C. Parker, *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 9, No. 2. (April 2015), pp. 175-187.

4. "Synaptic Variability in a Cortical Neuromorphic Circuit," Mohammad Mahvash and Alice C. Parker, Neural *Networks and Learning Systems, IEEE Transactions on*
Volume: 24, Issue: 3, 2013, Page(s): 397 - 409.

5. " Challenges for Brain Emulation: Why is it so Difficult?" Rick Cattell and Alice Parker, *Natural Intelligence, the INNS Magazine*, v. 1, issue 3, Spring/Summer 2012, pp. 17-31.

6. “Emulation of Neural Networks on a Nanoscale Architecture,” Mary M. Eshaghian-Wilner, Aaron Friesz, Alex Khitun, Shiva Navab, Alice C. Parker, Kang L. Wang, and Chongwu Zhou, special issue of the *Journal of Physics*: Conference Series, 2007, **61** 288-292.

7. “ Interconnect-based system-level energy and power prediction to guide architecture exploration,” Suhrid A, Wadekar, and Alice C. Parker, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Volume: 12, Issue: 4, April 2004, pp. 373 – 380.

8. “Automated Design of Hierarchical Intranets,” Sami Habib, Alice Parker, and Daniel Lee, *Computer Communications,* Vol. 25, No. 11-12, pp. 1065-1077, 2002.

9. "Taking Thermal Considerations into Account During High-Level Synthesis", J-P Weng and A. Parker, *VLSI Design*, Gordon and Breach Publishers, 1996.

10. "A Suboptimal Heterogeneous Mapping," M. Eshaghian, A. Parker and Y-C Wu, *Journal of High Performance Computing*, Vol. 3, No. 1, 1995, pp. 7-15.

11. "A Methodology and Design Tools to Support System-Level VLSI," K. Kucukcakar and A. Parker, *IEEE Transactions on VLSI*, 1995.

12. "Synthesis of Application-Specific Multiprocessor Systems including Memory Components", S. Prakash and A. Parker, invited paper, special issue, *Journal of VLSI Signal Processing*, 1994.

13. "SOS: Synthesis of Application-Specific Heterogeneous Multiprocessor Systems", S. Prakash and A. Parker, *Journal of Parallel and Distributed Computing*, December 1992, Vol. 16, pp. 338-351.

14. "Predicting System-Level Area and Delay for Pipelined and Nonpipelined Designs", Rajiv Jain, Nohbyung Park and Alice Parker, *IEEE Transactions on Computer-Aided Design*, Vol. 11, No. 8, pp. 955-965,August 1992.

15. "The ADAM Design Planning Engine", D. Knapp and A. Parker, *IEEE Transactions on Computer-Aided Design*, Vol. 10, #7, July1991, pages 829-846.

16. "MABAL: A Software Package for Module and Bus Allocation", with K. K. Kucukcakar and A. Parker, *International Journal of Computer Aided VLSI Design*, Vol. 2, No. 4, 1990, pp. 419-436

17. "The High-Level Synthesis of Digital Systems", M. McFarland, A. Parker and R. Camposano, *Proceedings of the IEEE*, Feb. 1990, pp. 301-318

18. “Techniques for Area Estimation of VLSI Layouts," F. Kurdahi and A. Parker, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, January 1989, pp. 81-92.

19. "Sehwa: A Software Package for Synthesis of Pipelines from Behavioral Specifications", N. Park and A. Parker, *IEEE Transactions on Computer-Aided Design*, Vol. 7, No. 3, March 1988, pp.356-370.

20. "Theory of Clocking for Maximum Execution Overlap of High-Speed Digital Systems", N. Park and A. Parker, *IEEE Transactions on Computers*, Vol. 37, No. 6, June 1988, pp. 678-690.

21. "Automating the VLSI Design Process using Expert Systems and Silicon Compilation," A. Parker and S. Hayati, invited paper, *Proceedings of the IEEE*, Vol. 75, No. 6, pp. 777-785, June 1987.

22. "Stochastic Models for Wireability Analysis of Gate Arrays," S. Sastry and A. Parker, *IEEE Transactions on Computer-Aided Design*, Jan 1986, pp. 52-65.

23. "Automatic Synthesis of Digital Systems," A. Parker, invited paper, *Design and Test*, Sept., 1984, pp. 75-81.

24. "A Representation for Shape Based on Peaks and Ridges in the Difference of Low-Pass Transform," James L. Crowley and A. Parker, *IEEE Transactions on Pattern Analysis and Machine Intelligence*, March, 1984, pp. 156-170.

25. "An Abstract Model of Behavior for Hardware Descriptions," Michael McFarland and A. Parker, *IEEE Transactions on Computers*, July, 1983, pp. 621-637.

26. "A Formal Method for the Specification, Analysis and Design of Register-Transfer Digital Logic," L. Hafer and A. Parker, *IEEE Transactions on Computer-Aided Design*, Jan. 1983, pp. 846-853, reprinted in *Advances in Circuits and Systems: Logic Synthesis for Integrated Circuit Design*, ed: A. Richard Newton, IEEE Press, pp. 121-134, 1987.

27. "Synthesis of Hardware for the Control of Digital Systems," A.W. Nagle, R. Cloutier and A. Parker, *IEEE Transactions on Computer-Aided Design*, Vol CAD-1, No. 4, Oct. 1982, pp. 201-212.

28. "Automated Synthesis of Digital Hardware," L. Hafer and A. Parker, *IEEE Transactions on Computers*, Feb. 1982, pp. 93-109.

29. "A Design Methodology and Computer Aids for Digital VLSI Systems, "Director, Siewiorek, Thomas, and Parker, *IEEE Transactions on Circuits and Systems*, vol. CAS-28, No. 7, July 1981, pp. 634-645, reprinted in *Advances in Circuits and Systems: Computer-Aided Design of Very Large Scale Integrated Circuits*, ed: Alberto L. Sangiovanni-Vincentelli, IEEE Press, pp. 86-96, 1987.

30. "SLIDE: An I/O Hardware Descriptive Language," Alice Parker and John Wallace. *IEEE Transactions on Computers*, June, 1981, pp. 423-439.

31. "The Automated Dictionary," A. Parker, M. Fox and D. Bebel, invited paper, *Computer*, April 1980, pp. 35-48.

32. "A Bus System for the Military Computer Family," with William Burr, et al., invited paper, *Computer*, April 1979, pp. 11-12.

Books

Women in Microelectronics, Edited by Alice C. Parker and Leda Lunardi, Springer, 2020.

Book Chapters

1. "Introduction," Alice Cline Parker and Leda Lunardi, *Women in Microelectronics*, Edited by Alice C. Parker and Leda Lunardi, Springer, 2020.

2. "From Silicon to the Brain using Microelectronics as a Bridge," Alice Cline Parker, *Women in Microelectronics*, Edited by Alice C. Parker and Leda Lunardi, Springer, 2020.

3. MODELING BRAIN DISORDERS IN SILICON NANOTECHNOLOGIES, Parker, A. C., Barzegarjalali, S., Yue, K., Lee, R. and Patil, S. (2016) in *Wireless Computing in Medicine: From Nano to Cloud with Ethical and Legal Implications* (ed M. M. Eshaghian-Wilner), John Wiley & Sons, Inc., Hoboken, NJ, USA. doi: 10.1002/9781118993620.ch14.

4. "Biomimetic Cortical Nanocircuits," Alice C. Parker, Aaron K. Friesz, and Ko-Chung Tseng, invited chapter in *Bio-inspired and Nano-scale Integrated Computing,* Edited by Mary M. Eshaghian-Wilner, Wiley, Inc., 2009.

5. "System-Level Design", Alice C. Parker, Yosef Tirat-Gefen and Suhrid A. Wadekar, invited chapter in the *IEEE/CRC VLSI Handbook*, CRC Press, 1999, updated second edition, 2006.

6. "Critical Path Analysis," S. Dey, Yosef Tirat-Gefen, A.C. Parker, and M. Potkonjak, invited chapter in *Encyclopedia of Electrical Engineering*, edited by J. Webster, John Wiley Inc., 1998.

7. "Synthesis in System Heterogeneous Computing," Shiv Prakash, Alice C. Parker, and J-C DeSouza Batista, *Heterogeneous Computing*, Artech House, Mary Mehrnoosh Eshaghian, Editor, 1996.

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9. "Unified System Construction (U.S.C.)", A. Parker, K. Kucukcakar, S. Prakash and J. Weng, invited chapter, in *High-Level VLSI Synthesis*, W. Wolf and R. Camposano, Editors, Kluwer, June, 1991.

10. "Automating the VLSI Design Process using Expert Systems and Silicon Compilation", A.C. Parker and S. Hayati, invited chapter, in *Expert Systems, A Software Methodology for Modern Applications*, IEEE Press, Peter G. Raeth, Editor, 1990, pp. 101-109.

11. "An Object-Oriented Approach to VLSI CAD", A.C. Parker, H. Afsarmanesh, D. Knapp and D. McLeod, invited chapter, *Readings in Object-Oriented Databases*, Morgan Kaufmann Publishers, Stanley B. Zdonik and David Maier, Editors, pp. 607-618, 1989.

12. "Data Path Synthesis of Pipelined Designs: Theoretical Foundations", N. Park, R. Jain and A.C. Parker, invited chapter, *Progress in Computer Aided VLSI Design, Volume III: Implementation*, Oct. 19, 1989, Ablex Publishing Corporation, George W. Zobrist, Editor.

13. "Interface and I/O Protocol Descriptions," A.C. Parker and N. Park, invited chapter, *Advances in CAD for VLSI, Vol. 7: Hardware Description Languages*, edited by R. Hartenstein, North Holland, pp. 111-136, 1985.

14. "Automated Synthesis of Digital Integrated Circuits," A. C. Parker, invited contribution, *IEEE ElectroTechnology Review 1984*, IEEE, 1984.

15. "Transfer Function Analysis of Picture Processing Operators," J. Crowley and A.C. Parker, In *Issues in Digital Image Processing*, Haralick and Simon, Sijthoff and Noordhof, The Netherlands, 1980, pp. 3-30.

Invited Papers published in Conference Proceedings

1. "Dendritic Computations, Dendritic Spiking and Dendritic Plasticity in Nanoelectronic Neurons," Chih-Chieh Hsu, Alice C. Parker and Jonathan Joshi, *IEEE Midwest Symposium on Circuits and Systems*, Seattle, Aug 2010.

2. "Towards Biomimetic Stereo Vision," Benjamin L. Raskob and Alice C. Parker, *IEEE NAECON*, August, 2010, IEEE.

3. "Towards a Nanoscale Artificial Cortex," A. Parker, A. Friesz and A. Pakdaman, Conference on Computer Design + Computing in nanotechnology, Las Vegas, June, 2006.

4. "Unified System Construction", A. Parker, C-T Chen and P. Gupta, *SASIMI Conference*, Nara, Japan, October 1993.

5. "Synthesis of Application-Specific Multiprocessor Systems Including Memory Components", S. Prakash and A. Parker, *Proceedings Int'l Conf. on Application-Specific Array Processors*, pp. 8-13, ACM/IEEE, July 1992.

6. "Impact of the Effects of Physical Design Characteristics in the Quality of Synthesized Designs", A. Parker, J. Weng, P. Gupta and A. Hussain, *Canadian Conference on VLSI Design*, Oct., 1990.

7. "Recent Advances in High-level Design for VLSI", A. Parker, *Proceedings of the 1988 Government Microcircuit Applications Conference*, November 1988.

8. "Design Style Selection for Digital Systems", R. Jain and A. Parker, *Techcon*, October 1988.

9. "Tutorial on High-Level Synthesis", M. McFarland, A. Parker and R. Camposano, *Proceedings of the 25th Design Automation Conference*, pp. 330-336, June 1988.

10. "Microprogramming - The Challenges of VLSI," A. Parker and W. Wilner, *Proceedings of the National Computer Conference*, pp. 63-68, May 1981.

11. "The Carnegie-Mellon University Design Automation System: Current Status and Future Direction," A. Parker, S. Director, D. Siewiorek and D. Thomas, *Proceedings, 1981International Symposium on Circuits and Systems*, Chicago, pp. 73-80, April 1981.

12. "The Application of a Hardware Descriptive Language for Design Automation," with L. Hafer, *Proceedings of the 3rd Jerusalem Conference on Information Technology*, August 6-9, 1978.

Papers Published in Conference Proceedings

1. "Neuromorphic Autonomous Spiking Encoding," Rami A. Alzahrani and Alice C. Parker, *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401769.

2. "Don't Lose Your Mind: Brain-Computer Interfaces, Autonomy, and the Necessity of Engineering Ethics," Madelyn Douglas and Alice C. Parker, 10th International IEEE/EMBS Conference on Neural Engineering (NER), May 2021.

3. Neuromorphic Circuits With Neural Modulation Enhancing the Information Content of Neural Signaling, Rami A. Alzahrani and Alice C. Parker, *ICONS 2020*, *International Conference on Neuromorphic Systems 2020*, July, 2020, Article No.19 Pages 1–8.

4. "Analog Neurons with Dopamine-Modulated STDP," Kun Yue and Alice C. Parker, *BIOCAS 2019 Biomedical Circuits and Systems Conference*, Nara, Japan, Oct. 17-19, 2019.

5. “Analog Neurons that Signal with Spiking Frequencies,” Kun Yue, Xiaoyu Wang, Jay Jadav, Akshay Vartak, and Alice C. Parker, *ICONS International Conference on Neuromorphic Systems*, Knoxville, TN, July 23-25, 2019.

6. “An Electronic Neuron with Input-Specific Spiking,” Rebecca K. Lee and Alice C. Parker, *IJCNN International Joint Conference on Neural Networks,* Budapest, Hungary, July 14-19, 2019

7. “Simulation Studies of Neuronal Modulation Using Magneto-electric Nanoparticles for Astrocyte Stimulation,” Kun Yue, Rebecca K. Lee, and Alice C. Parker, *9th International IEEE EMBS Conference on Neural Engineering*, San Francisco, CA, USA, March 20 - 23, 2019.

8. "Incorporating Astrocytes into Spiking Neuromorphic Designs using Dual-Gated Molybdenum Disulfide (MoS2) FETs," Kun Yue, Alice C. Parker, Han Wang, *18th IEEE International Conference on Nanotechnology*, Cork, Ireland, July 23-26, 2018.

9. “A Power-Efficient Biomimetic Intra-Branch Dendritic Adder,” Pezhman Mamdouh and Alice C. Parker, *IJCNN Proceedings*, May, 2017.

10. “*C. elegans* Neuromorphic Neural Network Exhibiting Undulating Locomotion,” N. Agarwal, N. Mehta, A. Parker and K. Ashouri, *IJCNN Proceedings*, May, 2017.

11. “A Switched-Capacitor Dendritic Arbor for Low-Power Neuromorphic Applications,” Pezhman Mamdouh and Alice C. Parker, *ISCAS Proceedings*, May, 2017.

12. Noisy Neuromorphic Neurons with RPG On-chip Noise Source,” Kun Yue and Alice C. Parker, *IJCNN Proceedings*, May, 2017.

13. “An Analog Neural Network that Learns Sudoku-Like Puzzle Rules,” Saeid Barzegarjalali and Alice C. Parker, *Future Technologies Conference FTC 2016*, San Francisco, Dec. 2016.

14. “A Bio-inspired Electronic Mechanism for Unsupervised Learning using Structural Plasticity,” Saeid Barzegarjalali and Alice C. Parker, *Future Technologies Conference FTC 2016*, San Francisco, Dec. 2016.

15. "A CMOS Circuit Implementation of Retrograde Signaling in Astrocyte-Neuron Networks", Rebecca Lee and Alice C. Parker, *IEEE 2016 Biomedical Circuits & Systems Conference BIOCAS*, Shanghai, October 17-19, 2016.

16. “Noisy Neuromorphic Circuit Modeling Obsessive-Compulsive Disorder,” Saeid Barzegarjalali, Kun Yue, and Alice C. Parker, *29th IEEE INTERNATIONAL SYSTEM-ON-CHIP CONFERENCE (SOCC 2016)*, Sept. 2016.

17. “Neuromorphic Circuit Modeling Directional Selectivity in the Visual Cortex”
    a. Saeid Barzegarjalali and Alice C. Parker, *IEEE Engineering in Medicine and Biology Society Conference(EMBC*'16*),* Aug. 2016.

18. “A Neuromorphic Circuit Mimicking Biological Short-Term Memory,” Saeid Barzegarjalali and Alice C. Parker, *IEEE Engineering in Medicine and Biology Society Conference* (*EMBC*'16), Aug. 2016.

19. "A Hybrid Neuromorphic Circuit Demonstrating Schizophrenic Symptoms," Saeid Barzegarjalali and Alice C. Parker, *BIOCAS 2015*, Oct. 22-24, Atlanta, GA.

20. "Neural Circuits for Touch-Induced Locomotion in *Caenorhabditis Elegans*," Sukanya Patil, Kaidi Zhou and Alice C Parker, the *International Joint Conference on Neural Networks,* Killarney, Ireland, July, 2015.

21. ``A Separated Carbon Nanotube Synapse,"Rebecca K. Lee, Jialu Zhang, Alice C. Parker, and Chongwu Zhou, IEEE EMBC Micro and Nanotechnology in Medicine Conference, Turtle Bay, 1 page paper, December 2014.

22. ``Nanoscale Neuromorphic Circuit to Model Demylination/Remyelination," Kun Yue and Alice C. Parker, IEEE EMBC Micro and Nanotechnology in Medicine Conference, Turtle Bay, 1 page paper, December 2014.

23. "Dynamic Spike Threshold and Nonlinear Dendritic Computation for Coincidence Detection in Neuromorphic Circuits," Chih-Chieh Hsu and Alice C. Parker, *36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'14)*, Chicago, Illinois, USA, August 26-30, 2014.

24. "Border Ownership in a Nano-Neuromorphic Circuit using Nonlinear Dendritic Computations," Chih-Chieh Hsu and Alice C. Parker, *IJCNN*, Beijing, China, July, 2014.

25. "Astrocyte on Neuronal Phase Synchrony in CMOS," Yilda Irizarry-Valle and Alice C. Parker, *IEEE ISCAS*, Melbourne, Australia, June, 2014.

26. "A Biomimetic Nanoelectronic Neuron with Enhanced Spike Timing," Chih-Chieh Hsu and Alice C. Parker, *IEEE ISCAS*, Melbourne, Australia, June 2014.

27. "An Adaptable CMOS Depressing Synapse with Detection of Changes in Input Spike Rate," Yilda Irrizarry-Valle, Alice C. Parker and Norberto Grzywacz, *IEEE LASCAS*, Feb., 2014, Santiago, Chile.

28. "Neuromorphic Network Implementation of the Somatosensory Cortex," Jonathan Joshi, Alice C. Parker and Tansu Celikel, *IEEE EMBC Conference on Neural Engineering*, Nov. 2013, San Diego.

29. "Biomimetic Non-linear CMOS Adder for Neuromorphic Circu**its,**" Xiahan Zhou, Yimu Guo, Alice C. Parker, Chih-Chieh Hsu and John Choma, *IEEE EMBC Conference on Neural Engineering*, Nov. 2013, San Diego.

30. "A CMOS Neuromorphic Approach to Emulate Neuro-Astrocyte Interactions," Yilda Irrizarry-Valle, Alice C. Parker and Jonathan Joshi, *IJCNN*, Aug. 2013.

31. "A Neuromorphic Circuit that Computes Differential Motion'", Ko-Chung Tseng and Alice C. Parker, IEEE MWSCAS, Boise, ID, Aug. 2012.

32. "Modeling Intrinsic Ion-Channel and Synaptic Variability in a Cortical Neuromorphic Circuit," Mohammad Mahvash, and Alice C. Parker, *BIOCAS 2011*, Nov. 2011.

33. "A Directionally-Selective Neuromorphic Circuit Based on Reciprocal Synapses in Starburst Amacrine Cells," Ko-Chung Tseng, Alice C. Parker, and Jonathan Joshi, *Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC),* Sept, 2011

34. "An in-silico glial microdomain to invoke excitability in cortical neural networks," Jonathan Joshi, Alice C. Parker, Ko-Chung Tseng, *2011 IEEE International Symposium on Circuits and Systems (ISCAS),* 15-18 May 2011, page(s): 681 - 684, Rio de Janeiro, Brazil.

35. "A biomimetic fabricated carbon nanotube synapse for prosthetic applications," Jon Joshi; Jialu Zhang; Chuan Wang; Chih-Chieh Hsu; Alice C. Parker.; Chongwu Zhou; and Udhay Ravishankar; *Life Science Systems and Applications Workshop (LiSSA), 2011 IEEE/NIH*, April 2011

36. "A Memristor SPICE Model for Designing Memristor Circuits," M. Mahvash and A. C. Parker, *IEEE Midwest Symposium on Circuits and Systems*, Seattle, Aug 2010, pages 989 - 992.

37. "A Carbon Nanotube Spiking Cortical Neuron with Tunable Refractory Period and Spiking Duration," Jonathan Joshi, Alice C. Parker, and Chih-Chieh Hsu, Third best paper award, *LASCAS Latin American Symposium on Circuits and Systems*, Feb., 2010, Iguazu Falls, Brazil.

38. "A Carbon Nanotube Cortical Neuron with Spike-Timing-Dependent Plasticity," Jonathan Joshi, Alice C. Parker, and Chih-Chieh Hsu, *Annual International Conf. of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Sept. 2-6, 2009, Minneapolis, Minn., page(s): 1651-1654.

39. "A Carbon Nanotube Cortical Neuron with Excitatory and Inhibitory Dendritic Computations," Jonathan Joshi, Chih-Chieh Hsu, Alice C. Parker and Pankaj Deshmukh, *IEEE/NIH Life Science Systems & Applications Wkshp 2009 (LiSSA '09),* April 9, 2009, Bethesda, Md., Pages: 133-136.

40. "A Hierarchical Artificial Retina Architecture," Alice C. Parker and Adi N. Azar, Bioengineered and Bioinspired Systems IV, edited by Ángel B. Rodríguez-Vázquez, Ricardo

A. Carmona-Galán,Gustavo Liñán-Cembrano, *Proc. of SPIE*, Vol. 7365, Dresden, Germany, 2009.

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42. " 3D Tree-Structured Object Tracking for Autonomous Ground Vehicles," Changsoo Jeong and Alice C. Parker, *Fourth Canadian Conference on Computer and Robot Vision (CRV07),* Montreal, May, 2007.

43. "Emulation of Neural Networks on a Nano-scale Spin-Wave Architecture," M. M. Eshaghian-Wilner, A. Friesz, A. Khitun, S. Navab, A. C. Parker, Kang L.Wang, C. Zhou, *International Conference on Nanoscience and Technology*, Basel, Switzerland, 2006.

44. "Exploring Network Topology Evolution Through Evolutionary Computations," Sami J. Habib, and Alice C. Parker*, Genetic and Evolutionary Computation Conference (GECCO-2006, 2006).*

45. "Managing Complexity in an Autonomous Vehicle," Joseph C. Bebel, Benjamin L. Raskob, Alice C. Parker and Donald J. Bebel, *Proceedings of PLAN 2006*, San Diego, California, 2006.

46. "Synthesizing complex multimedia network topologies using an evolutionary approach, "Sami J. Habib, and Alice C. Parker, *Congress on Evolutionary Computation, 2004* (CEC2004), Volume: 1, June 19-23, 2004 pp. 1193 –1200.

47. "NETCAP: A Capacity Planning Tool for Content Distribution Network Designs," S. Habib and A. Parker, In the *2003 Proceedings of International Symposium on Performance Evaluation of Computer and Telecommunication Systems (SPECTS 2003),* Montreal, Quebec, Canada.

48. S. Habib and A. Parker, "iCAD: A Rapid Prototyping CAD Tool for Intranet Design," In the *2003 Proceedings of the fourteenth IEEE International Workshop on Rapid System Prototyping* (RSP 2003), San Diego, California, USA.

49. "Computer-Aided System Integration Tool for Predicting Enterprise Network Evolution," S. Habib and A. Parker, *Proceedings of the 15th International Conference on Systems Engineering*, Las Vegas, Nevada, pp. 112-118, August, 2002.

50. "Automating Heterogeneous Intranet Design Including Data Management," S. Habib and A. Parker, *Proceedings of The 6th World Multiconference on Systemics, Cybernetics and Informatics*, Orlando, Fla., Vol. XVI, Computer Science III, pp. 343-348, July, 2002.

51. "Automated Design of Hierarchical Intranets," S. Habib, A. C. Parker, and D. C. Lee, 2001 International Symposium on Performance Evaluation of Computer and Telecommunication Systems, July, 2001, 383-390.

52. “Computer-Aided System Integration for Data-Intensive Multimedia Applications,” S. Habib and A. Parker, *ACM Multimedia 2000*, Nov., 2000, pp. 379-381.

53. "FREEDOM: Statistical Behavioral Estimation of System Energy and Power," S.A. Wadekar, A. C. Parker and C.P. Ravikumar, in *Proc. Eleventh International Conference on VLSI Design*, pp. 30-36, Jan. 1998.

54. "Accuracy Sensitive Word-Length Selection for Algorithm Optimization," S.A. Wadekar and A.C. Parker, in *Proc. International Conf. on Circuit Design*, pp. 54-61, Oct. 1998.

55. "Algorithm-Level Verification of Arithmetic-Intensive Application-Specific Hardware Designs for Computation Accuracy," S.A. Wadekar and A. C. Parker, in *Digest IEEE International High Level Design Validation and Test Workshop*, pp. 80-87, Nov. 1998.

56. "An Evolutionary Approach to System Redesign", D.H. Heo, C.P. Ravikumar, and A. Parker, *Proceedings of the 11th International Conference on VLSI Design*, India, 1998, PP.359-362.

57. "Specification and Validation of System Level Designs" Diogenes C. Silva and Alice C. Parker, *International Workshop on Logic and Architecture Synthesis - IWLAS '97*, Grenoble, France, December 16-18 1997, pp. 255-264.

58. "Incorporating Imprecise Computation into System-level Design of Application-specific Heterogeneous Multiprocessors", 34th DAC proceedings, Yosef G. Tirat-Gefen, Diogenes C. Silva and Alice C. Parker, DAC'97 - *Proceedings of the 34th. Design Automation Conference*, Anaheim, CA June 9-13, 1997.

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60. "Rapid Synthesis of Multi-Chip Systems", D.H. Heo, C.P. Ravikumar, and A. Parker, *Proceedings of the 10th International Conference on VLSI Design*, Hyderabad, India, Jan. 1997, pp.62-68.

61. "Synthesis of Optimal MCM-Based Systems," D.H. Heo, C.P. Ravikumar, and A. Parker, *InterPACK'97*, Kohala Coast, Island of Hawaii, USA, 1997. EEP-vol. 19-1,Advances in electronic packaging-1997,Vol.1, ACME 1997,PP.843-850.

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80. "CHOP: A Constraint-Driven System-Level Partitioner", K. Kucukcakar and A. Parker, in *Proceedings of 28th Design Automation Conference*, ACM/IEEE, June, 1991.

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88. "Area-Time Model for Synthesis of Non-Pipelined Designs", with R. Jain and M. Mlinar, *Proceedings of the 1988 International Conference on Computer-Aided Design*, pp. 48-51, November 1988.

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90. "The POTATO Chip Architecture: A Study in Tradeoffs for Signal Processing Chip design", with B. Sharma, R. Jain, M. Breuer, C. Raghavendra and C.Y. Tseng, *Proceedings of the 1988 IEEE International Conference on Computer Design: VLSI in Computers and Processors*, Rye Brook, New York, pp. 508-513, October 1988.

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93. "Phrasal Analysis of Long Noun Sequences", with Y. Arens and J. Granacki, *Association for Computational Linguistics Annual Meeting*, July, 1987.

94. "PHRAN - Span: A Natural Language Interface for System Specifications", J. Granacki and A. Parker, *Proceedings of the 24th ACM/IEEE Design Automation Conference*, pp. 416-422, June, 1987.

95. "REAL: A Program for Register Allocation", F. Kurdahi and A. Parker, *Proceedings of the 24th ACM/IEEE Design Automation Conference*, June, 1987.

96. "Predicting Area - Time Tradeoffs for Pipelined Design," with R. Jain and N. Park, *Proceedings of the 24th ACM/IEEE Design Automation Conference*, pp. 35-41, June, 1987.

97. "Information Management for VLSI/CAD", with H. Afsarmanesh, D. Knapp, and D. McLeod, *Proceedings of the ICCD '86 IEEE International Conference on Computer Design VLSI IN Computers and Processors*, pp. 476-481, October 1986.

98. "A Design Utility Manager: The ADAM Planning Engine", D. Knapp and A. Parker, *Proceedings of the 23rd Design Automation Conference*, pp. 48-54, June, 1986.

99. "SEHWA: 'A Program for Synthesis of Pipelines", N. Park and A. Parker, in *25 Years of Electronic Design Automation*, IEEE and ACM, June 1988, reprinted from *Proceedings of the 23rd Design Automation Conference*, pp. 356-370, June, 1986.

100. "MAHA: A Program for Datapath Synthesis", with J. Pizarro, M. Mlinar, *Proceedings of the 23rd Design Automation Conference*, pp. 461-466, June, 1986.

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102. "A Natural Language Interface for Specifying Digital Systems", J. Granacki and A. Parker, *Proceedings of the First International Conference on Application of Artificial Intelligence to Engineering Problems*, Southampton England, April 15-18, 1986.

103. "A Unified Representation for Design Information", with D. Knapp, *Proceedings of the IFIP Conference on Hardware Description Languages*," August, 1985.

104. "An Extensible Object-Oriented Approach to Databases for VLSI/CAD", with H. Afsarmanesh, D. Knapp and D. McLeod, *Proceedings of the 11th International Conference on Very Large Data Bases*, Stockholm, pp. 164-166, August 21-23 1985.

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109. "On the Relation between Wire Length Distribution and Placement of Logic on Master Slice IC's," S. Sastry and A. Parker, *Proceedings of the 21st Design Automation Conference*, pp. 710-711, June 1984.

110. "An Expert Synthesis System," with D. Knapp and J. Granacki, *Proceedings of the International Conference on Computer-Aided Design*, pp. 164-165, 1983.

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112. "The Effect of Register-Transfer Design Tradeoffs on Chip Area and Performance," with J. Granacki, *Proceedings of the 20th Design Automation Conference*, pp. 419-424, June 1983.

113. "A Database System for Procedural VLSI Design," with K. Wu, *Proceedings of 1983 Symposium on VLSI Technology, Systems, and Applications*, Taiwan, 1983.

114. "A Technique for Automatically Producing Optimized Digital Designs," with D. Dervos, *MELECON '83, Mediterranean Electrotechnical Conference*, pp. B204-B205, May 1983 Proceedings.

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121. "SLIDE: An I/O Hardware Descriptive Language," with John Wallace, *Proceedings of 1979 International Symposium on Computer Hardware Descriptive Languages*, pp. 423-439, October 1979.

122. "ISPS: A Retrospective View," with D. Thomas S. Crocker and R. Cattell, *Proceedings of International Symposium on Computer Hardware Descriptive Languages*, pp. 21-27, October 1979.

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125. "The Analysis, Synthesis and Evaluation of Local Measures for Discrimination and Segmentation of Textured Regions," with J. Crowley, *Proceedings of the IEEE Pattern Recognition and Image Processing Conference*, Chicago, pp. 372-378, June 1978.

126. "Register-Transfer Level Digital Design Automation: The Allocation Process," with L. Hafer, *Proceedings of the 15th Design Automation Conference*, pp. 213-219, June 1978.

127. "Description and Simulation of Microcode Execution," *Proceedings of the Fifth Annual Computer Architecture Symposium*, pp. 159-165, April 1978.

128. "Linear Analysis of Picture Processing Operators," with J. Crowley, *Proceedings of the COMPCON*, pp. 320-324, Spring 1978.

129. "Digital Interface Description," *Proceedings of the COMPCON*, Spring 1978.

130. "Envelope Control with an Optical Keyboard," with P. Dworak. *Proceedings of the Second Annual Computer Music Conference*, San Diego, October 1977.

131. "Hardware/Software Tradeoffs in a Variable Word Width, Variable Queue Length Buffer Memory," with A. Nagle, *Proceedings of the 4th Annual Symposium on Computer Architecture*, pp. 159-163, March 1977.

132. "The Design and Implementation of a Real-Time Sound Generation System," with others. *Proceedings of the 4th Annual Symposium on Computer Architecture*, pp. 153-158, March 1977.

133. "Educational and Industrial Applications of Register Transfer Modules," with D. Siewiorek., Euromicro, *Proceedings of the Second Symposium on Microarchitecture*, pp. 221-231, October 1976.

134. "Social Impacts of Advanced Domestic Load Managements Systems," with G. Morgan, S. Talukdar and D. Tuma, *Frontiers of Power Technology Conference*, pp. 153-158, October 1976.

135. "An Input Interface for the Real-Time Control of Musical Parameters," with P. Dworak. *Proceedings of the First International Conference on Computer Music*, MIT, pp. 221-231, October 1976.

136. "An Input Interface for a Real-Time Digital Sound Generation System," with Paul Dworak. *Proceedings of the Third Annual Symposium on Computer Architecture*, pp. 68-73, January 1976.

137. "A Language for the Specification of Digital Interfacing Problems," with James W. Gault. *Proceedings of the 1975 International Symposium on Computer Hardware Descriptive Languages and Their Applications*, New York, pp. 85-90, September 1975.

138. "Digital Analysis of Speech," presented at *IEEE Region III Student Paper Competition*, 1970, Gainesville, FL,

Opinion

1. "The Elephant in the Mirror: Bridging the Brain's Explanatory Gap of Consciousness," Jasmine A. Berry and Alice C. Parker, *Frontiers in Systems Neuroscience* | www.frontiersin.org, January 2017 | Volume 10 | Article 108.

COURSES TAUGHT

- CMOS NanoNeuromorphic Circuits (Designed)
- Fundamentals of Electrical Engineering
- Introduction to Digital Systems, Seminar in Computer Engineering
- Computer Structures
- Fundamentals of Control
- Computer Systems Architecture
- Advanced Computer Systems
- Computer Architecture
- Design Automation
- Advanced Design Automation (Designed)
- VLSI System Design
- MOS VLSI Circuit Design (Designed)
- Alternative Energy Honors Project Course (Designed)

PROFESSIONAL ACTIVITIES

- **Life Fellow of IEEE**, Member of ACM, Eta Kappa Nu, Sigma Xi, Phi Kappa Phi, Tau Beta Pi, Society of Women Engineers (SWE).

- IEEE Computer Society Board of Governors 1994-96

- Academic Senate President, University of Southern California, elected 1994, served briefly then administrative responsibilities were assumed.

- Academic Senate Vice President, University of Southern California, 1993-94, Executive Board member 1991-93.

- Program Chairman, Eleventh Annual Microprogramming Workshop, November 1978.

- Reviewer: NSF Loci Program, IEEE Transactions on Computers, Computer Magazine, Journal of Design Automation and Fault-tolerant Computing, Design Automation Conferences, Computer Architecture Symposium, Hardware Descriptive Language Conferences, NSF, Transactions on Computer-Aided Design, Transactions on Circuits and Systems, Nature Nanotechnology, Cerebral Cortex, IEEE Transactions on Biomedical Circuits and Systems.

- ACM National Lecturer, 1979-80; Service Award 1990.

- Formerly on the Editorial Board," Integration, The VLSI Journal," North-Holland Publishers; "Journal of AI in Engineering," Computational Mechanics Publishers; "IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems", and" CAD/CAM Abstracts"

- Former member and Research Reviews Editor," Design and Test Magazine"

- Former Series Editor, CRC Press.

- IEEE High-Level Synthesis Workshop program committee 1989 and 1992, local arrangements 1983, program chairman 1985.

- IEEE International Conference on System-Level Synthesis program committee, 2000.

- Treasurer, ACM Special Interest Group on Microprogramming, 1979-81.

- Vice-Chairman 1981-83.

- Treasurer, ACM Special Interest Group on Design Automation, 1983-86.

- Member, ACM Computing Reviews Category Revision Committee, 1979-81.

- Program Committee Member, Fifth International Conference on Computer Hardware Description Languages and their Applications, Germany, September 1981, International Conference on Computer Aided Design, 1984-91, Design Automation Conference, 1986,

Applications of Artificial Intelligence in Engineering, 1988, Hardware Software CoDesign Workshop, 1992.

- Listed in Who's Who in Technology Today, 2nd Edition, Who's Who in Frontier Science and Technology, Who's Who of American Women, Who's Who in the West, World Who's Who of Women, Who's Who in America (2002), American Men and Women of Science 21st edition, and others.

- Member, Technical Advisory Board, CAD Framework Initiative.

- *Distinguished Lecturer,* Stanford, U., 1984-85.

- *Distinguished Lecturer,* Case Western Reserve University, 1990.

Consulting

Xerox Corporation, Information Sciences Institute, Digital Equipment Corporation, The Aerospace Corporation, Hewlett-Packard, National Institute of Education, Westinghouse Electric Corporation, United States Army, Electronics Command (Ft. Monmouth), Hughes Aircraft, General Electric, Synopsys, Teledyne, Exploration Institute.

Funding Since 1983

- Principal Investigator, "A *NeuRoBot* that Learns Locomotion Online and Generalizes/Learns Variations Autonomously without Forgetting," DARPA, 2018-2019, $499,897.

- Principal Investigator, "Biomimetic Cortical Nanocircuits, " National Science Foundation, 2007-2010, $359,997.

- Principal Investigator," System-Level Design Technology for Multi-Chip Designs, " Defense Advance Projects Research Agency, 1993-1998, $709,044.

- Awardee, NSF Faculty Awards for Women in Science and Engineering, 1991-98, $250,000.

- Principal Investigator, "System-Level Synthesis", Semiconductor Research Corporation, 1989-92, $355,530.

- Faculty Investigator," CAD Framework and Tools for the Synthesis of Complex Testable Digital Systems ", Defense Advance Projects Research Agency, 1990-93, (M. Breuer, P.I.), $2.2M.

- Principal Investigator, “System-Level-Level Tools for the ADAM Advanced Design AutoMation System," U.S. Navy 1987-91, $1,045,000.

- Principal Investigator," Vertically-Integrated VLSI Design for Signal Processing," Semiconductor Research Corporation, 1987-89, $510,000.

- Principal Investigator," Designing VLSI Circuits which Emulate Neurons", USC-FRIF 1990-92, $15,000.

- Principal Investigator, "VLSI CAD System", MCC 1985-88, $60,000.

- Faculty Investigator, "A knowledge Based System for the Design of Testable Systems", DARPA 1986-90, $300,000 (Breuer, P.I.).

- Principal Investigator, "VLSI CAD System", GE 1986-90, $25,000.

- Faculty Investigator, "An Object Oriented Environment to Integrate Design and Test of VLSI Circuits", AT&T 1988-90, $50,000 (M. A. Breuer P.I.).

- Principal Investigator, "Formal Models of Hardware and Their Applications to VLSI Design Automation," U.S. Army Research Office 1983-86, $244,502.

- Principal Investigator, "The ADAM VLSI Design System", National Science Foundation 1984-86, $420,000.

- Principal Investigator, "A Prototype System for Logical Error Detection," International Business Machines Corporation 1981-84, $150,000.

Distinguished Ph.D. Students

- Michael McFarland, President, Gregorian Foundation, and Former President, Holy Cross University
- Nohbyung Park, Senior Vice President, Samsung
- David Knapp, CEO, Get-to-Chip (sold to Cadence)
- James Crowley, Professor, Institut National Polytechnique de Grenoble, Chevalier de l'Ordre National du Mérite
- Sarma Vrudhula, Chaired Professor, Arizona State University
- John Granacki, Division Director, USC Information Sciences Institute

Complete student information can be found at https://ceng.usc.edu/~parker/students.shtml and https://ceng.usc.edu/~parker/DissertationResearchAreas.html