UNIVERSITY OF SOUTHERN CALIFORNIA COMPUTER ENGINEERING

SCREENING EXAMINATION ELECTIVE

EE 653

Advanced Topics in Microarchitecture

BASIC READING

Book: Dubois, Annavaram and Stenström',"Parallel Computer Organization and Design"

Papers:

[1] V. Agarwal, M.S. Hrishikesh, S.W. Keckler, and D. Burger. Clock rate versus ipc: the end of the road for conventional microarchitectures. Proceedings of the 27th International Symposium on Computer Architecture, 2000, pages 248-259.

[2] C. Gniady, B. Falsafi , and T.N. Vijaykumar. Is sc+ilp=rc? Proceedings of the 26th International Symposium on Computer Architecture, 1999, pages 162-171, 1999.

[3] E. Rotenberg, S. Bennett, and J.E. Smith. Trace cache: a low latency approach to high bandwidth instruction fetching. MICRO-29. Proceedings of the 29th Annual IEEE/ACM International Symposium on microarchitecture, pages 24-34, Dec 1996.

[4] S.S Mukherjee, C. Weaver, J. Emer, S.K. Reinhardt, and T.Austin. A systematic methodology to compute the architectural vulnerability factors for a high-performance microprocessor. Proceedings of the 36th Annual International Symposium on Microarchitecture, pages 29-40, Dec 2003.

[5] T. Sherwood, E. Perelman, G. Hamerly, and B. Calder. Automatically characterizing large scale program behavior. In Proceedings of the 10th International Conference on Architectural Support for Programming Languages and Operating Systems, pages 45-57.

[6] K. E. Moore, J. Bobba, M. J. Moravan, M. D. Hill & D. A. Wood. LogTM: Log-based Transactional Memory. In proceedings of the12th Annual International Symposium on High Performance Computer Architecture (HPCA-12), 2006.

[7] L. Hammond et al. Transactional Memory Coherence and Consistency. In Proceedings of the 31st International Symposium on Computer Architecture, 2004.

[8] L. Hammond, M. Willey, and K. Olukotun. Data speculation support for a chip multiprocessor. SIGOPS Operating Systems Review, 32(5):58-69, 1998.

[9] H. Akkary, R. Rajwar, and S. Srnivasan. Checkpoint processing and recovery: Towards scalable large instruction window processors. 36th International Symposium on Micro-architecture (MICRO-36), 2003.

[10] J. Chang and G. Sohi. Cooperative caching for chip multiprocessors. Proceedings of the 33rd International Symposium on Computer Architecture (ISCA), 2006.

[11] M. K. Qureshi, G. H. Loh: Fundamental Latency Trade-off in Architecting DRAM Caches: Outperforming Impractical SRAM-Tags with a Simple and Practical Design. MICRO 2012, pp. 235-246