THE AUTOMATIC DESIGN OF TESTABLE CIRCUITS*

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ABSTRACT

In this report we extended the previous work on testability measures for digital circuits, as represented by the scoap system. In our work we employ a new way for computing the testability measures (costs), namely, we formulate the problem as an ILP. By so doing we can achieve results never before attained, namely automatic design for testability. That is, the system will automatically add test logic so that the desired testability constraints and goals can be achieved.

1. Introduction

Because of the growing complexity of digital circuits, design for testability is essential [GRA80, WIL73]. Rutman [RUT72] and Stephenson [STE74] introduced techniques for measuring the testability of digital circuits. Rutman's work was further extended by Breuer [BRE77, 78, 79] and the results of this work were further developed and implemented in the scoap program [GOL78, 79, 80]. This program, like other testability programs [BEN80], [DUS78], [GRA79], [KOV79], [LON79], calculates the relative observability and controllability of the various nodes in a circuit using a heuristic procedure. Based upon these values, the designer is supposed to redesign his circuit in order to get better testability values. In general this can be a very complex process.

In this paper we show how to formulate the calculation of the testability measures as an integer linear program (ILP). We also show how to include additional constraints and objective criteria so that the program can automatically resynthesize the circuit. Similar concepts have been discussed in [PAR81, PAR82].

2. Testability Measures

Though our technique can apply to several different testability measures, for simplicity we will employ the one introduced by Rutman.

Definitions:

$C\delta_i$ – the complexity (difficulty or cost) of controlling (bringing) line i to the value δ, $\delta \in \{0,1\}$ by placing values on the primary inputs.

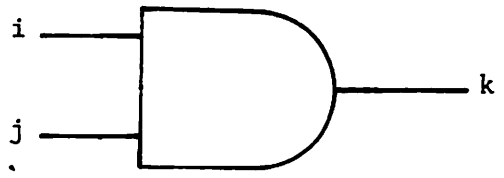
D_i – the complexity of observing (deducing) the value of line i by observing the values on the primary outputs.

The boundary conditions are:

$C\delta_i$ = 0 for all primary input lines i.

D_i = 0 for all primary output lines i.

The values of D_i and $C\delta_i$ for internal nodes are computed as follows. (We will illustrate the concept for only an AND gate.)

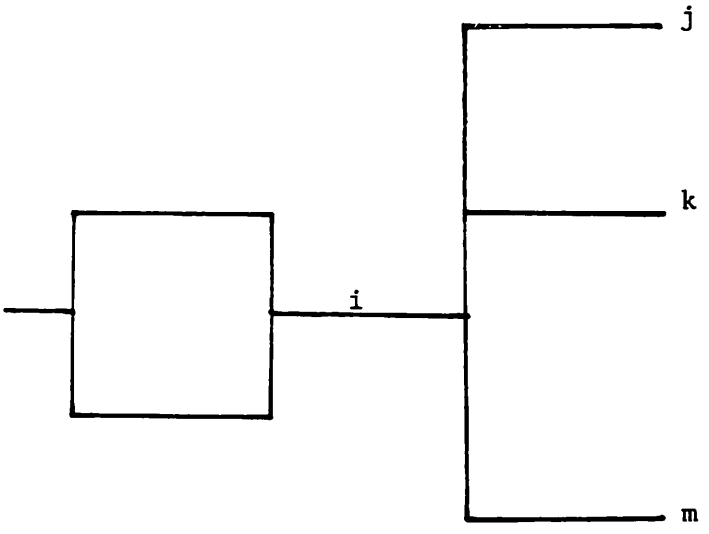


$$C1_k = 1 + C1_i + C1_j \quad (1)$$

$$CO_k = 1 + \min \{CO_i, CO_j\}$$

$$D_j = 1 + D_k + C1_i$$

For a fan-out line as shown below



$$D_i = \min(D_j, D_k, D_m)$$

For sequential circuits the values of $C\delta_i$ and D_i for a feedback line i are initially set to some large (maximum) value M.

The value of all testability factors $C\delta_i$ and D_i in a circuit can be computed in an iterative fashion as described by Rutman [RUT72].

3. ILP Formulation

We will now show how the computation of the testability values in a circuit can be formulated as an ILP. From (1) the computation requires the ability to add as well as find the minimum value of a set of quantities. We need only concern ourselves with the latter problem.

Let $\delta \in \{0,1\}$. Then min (x,y) can be expressed as an ILP as follows, where M is a large constant.

$$x - y \leq M\delta \tag{2a}$$

$$x \leq \alpha + M(1-\delta) \tag{2b}$$

$$y \leq \beta + M\delta \tag{2c}$$

$$Z(\min) = Z' + \alpha + \beta + \delta \tag{2d}$$

Assume $x > y$. Then $\delta = 1$ (2a) and from (2b) $x \leq \alpha$ and from (2c) $y \leq M$. By minimizing $\alpha + \beta$ we obtain $\alpha = x$ and $\beta = 0$. Similarly, if $x \leq y$, then $\delta = 0$ and $\alpha = 0$ and $\beta = y$. Thus

$$\alpha + \beta = \min(x,y).$$

Hence an equation of the form

$$C = 1 + \min(x,y)$$

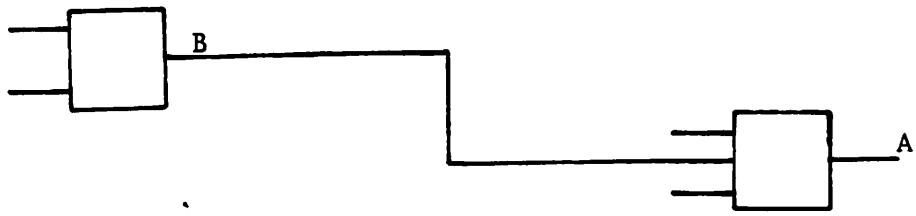
takes the ILP form

$$C = 1 + \alpha + \beta$$

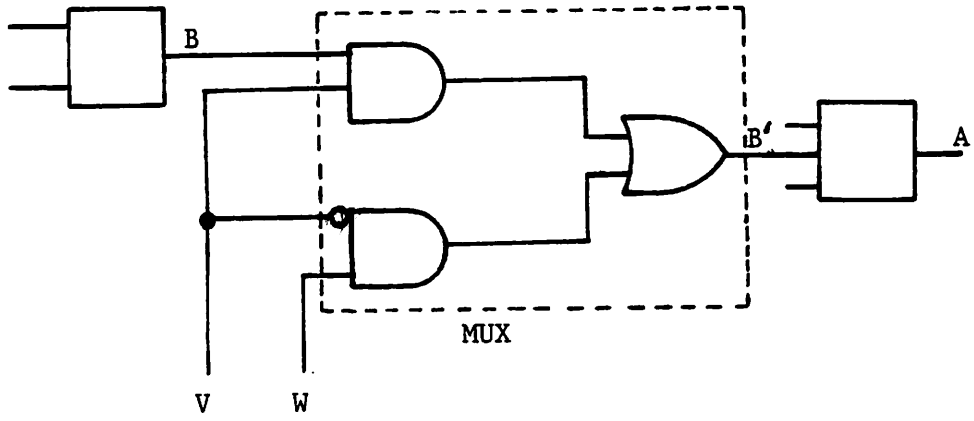
Controlability Circuitry

A node can be made more controllable by adding an AND gate (0-control) or an OR gate (1-control) or both.

Example:



Original Circuit



Modified Circuit

When V = 1 the circuit operates in its original way (B' = B), while if V = 0, B' = W (the injected line value).

The ILP can automatically add such test circuitry when required. The formulation is as follows.

Let $p \in \{0,1\}$ and $\Delta \in \{0,M\}$.

p = 0 implies test circuit not used

p = 1 implies test circuit used

Set $\Delta = (1-p)\ M$

Then p = 0 implies $\Delta = M$
p = 1 implies $\Delta = 0$

Set $CO_{B'} = \min\ (CO_B, \Delta)$

$C1_{B'} = \min\ (C1_B, \Delta)$

We modify the objective function to be of the form

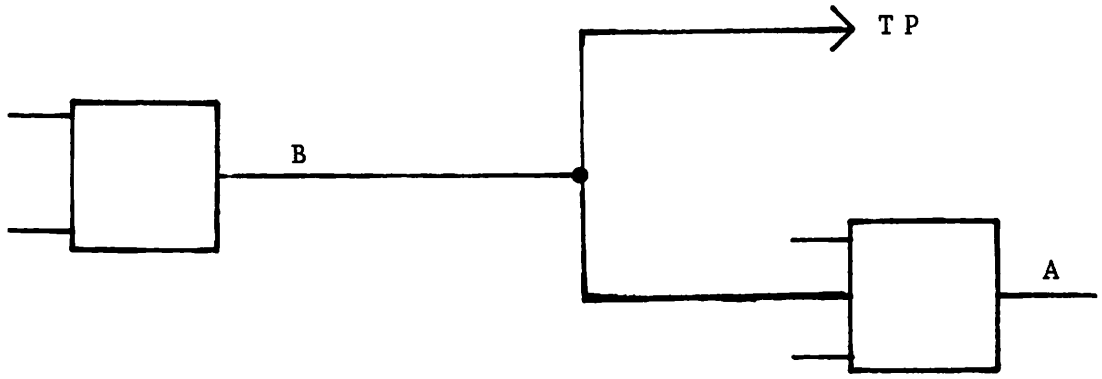
$Z(\min) = . \ . \ . \ + K_1 p$

where K_1 is the relative cost of a test circuit.

If there are numerous potential test circuits which can be added, then the number of circuits added can be constrained via the inequality

$$\sum_i p_i \leq K_2 \text{ (upper bound)}.$$

To aid in observability, a test point can be added, as shown below.



Now $D_{B'} = \min\ (D_B, \Delta)$

The testability values can be forced to be arbitrarily small, at the expense of adding controlability and observability logic, by adding constraints of the form

$$CO_i \leq K_3$$

$$C1_i \leq K_4$$

$$D_i \leq K_5$$

The objective function is of the form.

$$Z(min) = K_6 \sum_i (CO_i + C1_i + D_i) \quad \text{testability measures}$$

$$+ K_7 \sum_i (\alpha_i + \beta + \delta_i) \quad \text{min function}$$

$$+ K_1 \sum_i p_i \quad \text{testability logic}$$

The selection of the values of K_6, K_7 and K_1 control the solution obtained. For example, if K_1 is very large compared to K_6, no testability logic will be added since the reduction in the CO, C1 and D terms may not warrant the cost of the added circuitry.

Numerous other constraints can be added to this formulation to control various aspects of the design.

A system for implementing this technique is currently under development.

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