ERROR DETECTION IN SEQUENTIAL CIRCUITS USING ROVING EMULATION AS A DETECTION MECHANISM

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Abstract

The probability of detecting a fault in a sequential circuit using the roving emulation (RE) as a testing mechanism is evaluated . We define the probability of detection for sequential circuits (PD) as the average probability of detecting a fault as a function of the number of random input vectors applied .

In this report we present a new method for evaluating PD . Both Moore and Mealy type synchronous sequential circuits are considered . We consider circuits consisting of D flip-flops . The detection probability is needed in order to evaluate the expected value of the error latency for systems containing sequential circuits and being tested via the roving emulation process . The results are illustrated for a simple sequential circuit .

I. Introduction

Due to the nature of sequential circuits the state and output vectors are not independent of previously applied inputs . This attribute is due to the feedback lines in the circuit . There are two types of sequential circuits . A Moore type machine is one in which the output of the circuit is associated with only the state of the machine . A Mealy type machine is one in which the output is a function of the input and the present state . Furthermore sequential circuits may be classified as synchronous or asynchronous . In the former, circuit inputs are allowed to change only during a certain period when the clock disables the circuit's flip-flops and prevents it from changing state . On the other hand, asynchronous circuits are designed to operate without a synchronizing clock .

In this report we will consider both Mealy and Moore type synchronous sequential circuits . We will evaluate the probability of detecting a fault in a sequential circuit as a function of the number of random input vectors (m) applied . This information is required in order to determine the error latency time using roving emulation[4]. We note in this analysis that due to the ability of the roving emulator to obtain the initial state of the sequential circuit , there will be no need for a synchronizing sequence or reset line in order to initialize the circuit to a known state .

Previous researchers have also considered the problem posed in this report . Shedletsky and McCluskey [1] assumed the existence of synchronizing sequence . Losq[2]assumed that both the circuit under test and the known fault free circuit can be initialized to the same state after the application of a long sequence of random inputs . The same assumption was made by David[3].

Detection of failures in sequential circuits using the RE as a testing mechanism can be accomplished in two different ways . The first one occurs when we have a discrepancy between the actual output of the circuit and the output of the simulated circuit . This detection is achieved during the simulation of the circuit operation . The second one occurs after the simulation process is complete, when we compare the final state of the device obtained during the second state dump with the final state obtained from its simulated counterpart . The second form of detection can be disregarded if the interruption of the system operation is too costly in terms of system performance degradation .

In our analysis we assume that the clock input is fault free . Random inputs are applied to the circuit according to a known probability distribution . After each clock pulse we obtain an output vector and a possible change in the state variables . In this report the clock rate is not considered because we evaluate PD as a function of the number of input vectors .

In section II we present our analysis for both Moore and Mealy type circuit . We will divide the sequential circuit into three partitions and present methods to obtain each partition parameters . These parameters are used to obtain the PD of the circuit given a certain failure probability for each partition . In section III we will illustrate our results on a simple sequential circuit . We will evaluate its parameters and calculate its probability of detection as a function of m .

II. Synchronous Sequential Circuits

From the RE device operation we know that there are four main stages in device testing . The first stage is the dumping of the initial state so that we can have our simulation model start in the same state as the circuit under test . Then the opening of the window occurs , in which we capture all the input and output vectors to the particular device under test. Then we have the final state dump . Finally we have the time needed to simulate the device . We note that all of the detection process is done in the final stage, and can be separated into two parts . The first part is the comparison of the output obtained during the opening of the window with the output obtained from simulation . The second part is achieved by comparing the final state of the actual and the simulated device . There are thus two source of detection . Figure 1 shows one cycle of this testing process .

Before we evaluate the detection probability we will define some parameters for combinational and sequential circuits .

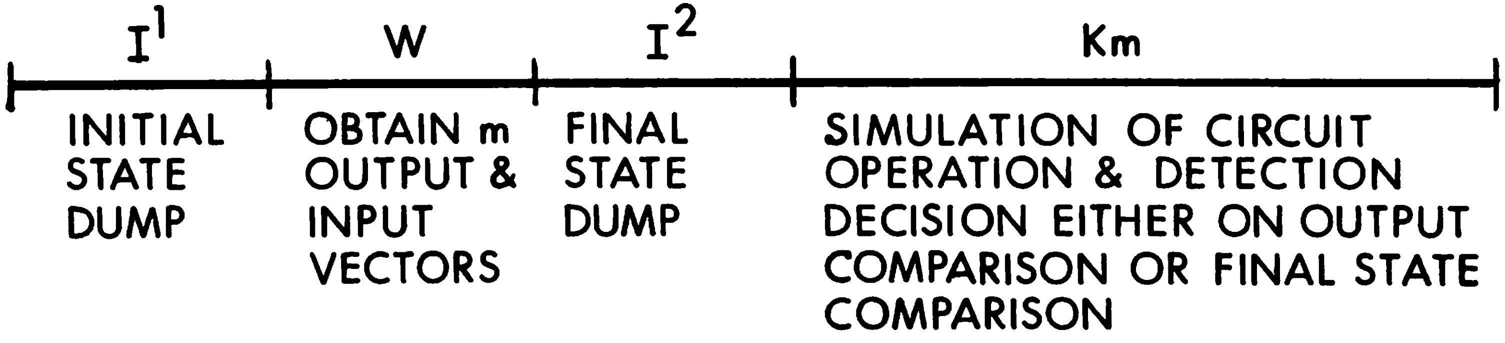
I1
W
I2
Km
INITIAL STATE DUMP
OBTAIN m OUTPUT & INPUT VECTORS
FINAL STATE DUMP
SIMULATION OF CIRCUIT OPERATION & DETECTION DECISION EITHER ON OUTPUT COMPARISON OR FINAL STATE COMPARISON

Fig. 1. A testing cycle

Definition 1

Let C_1 and C_2 be two combinational circuits . Let D_1 and D_2 be the input probability distributions for C_1 and C_2 respectively . The average propagation probability is the probability that two different random inputs chosen from the distributions D_1 and D_2 yield different outputs .

Let X_1 (Z_1) and X_2(Z_2) be the input (output) sets which contains all possible input (output) vectors of circuits C_1 and C_2 respectively . Let D_1 and D_2 be the probability distributions for the input sets X_1 and X_2 respectively . Two different input vectors are said to be equivalent (nonequivalent) if they produce the same (different) output vectors . Hence, for any two different input vectors chosen randomly from X_1 and X_2 the average propagation probability will be equal to the probability that the two vectors are nonequivalent . Let $x_{1i} \in X_1$ and $x_{2j} \in X_2$, where $1 \leq i \leq X_1$ and $1 \leq j \leq X_2$. Let C_1 and C_2 realize the Boolean functions f_1 and f_2 respectively . Then the average propagation probability is given by the following :

$$\frac{\text{the probability of applying nonequivalent different inputs}}{\text{the probability of applying different inputs}}$$

$$= \frac{\sum_{i=1}^{|X_1|} \sum_{j} p_1(x_{1i}) p_2(x_{2j})}{\sum_{i=1}^{|X_1|} \sum_{K} p_1(x_{1i}) p_2(x_{2K})} \qquad (1)$$

where the inner summation in the numerator is taken over all j such that $f_1(x_{1i}) = f_2(x_{2j})$, and $x_{1i} = x_{2j}$. The inner summation in the denominator is taken over all k such that $x_{1i} = x_{2K}$. $p_1(x_{1i})$ and

$p_2(x_{2j})$ are the probabilities of applying the input x_{1i} and x_{2j} to C_1 and C_2 respectively .

Definition 2

Let C_1 and C_2 be two combinational circuits . Each circuit has n input lines . Let $x_i = (x_{i1}, x_{i2}, \ldots . , x_{in})$ and $x_j = (x_{j1}, x_{j2}, \ldots . , x_{jn})$ be two input vectors to the circuit C and C respectively . The pair x_i and x_j are said to be constrained in $\beta < n$ lines iff $x_{i\sigma_k} = x_{j\sigma_k}$,where $1 \leqslant \sigma_k \leqslant n$ and $k = 1, 2, \ldots , \beta$.

Definition 3

Let C_1 and C_2 be two combinational circuits . Let D_1 and D_2 be the input probability distributions for C_1 and C_2 respectively . The average constrained propagation probability is the probability that two different constrained random inputs chosen from the distributions D_1 and D_2 yield different outputs .

The input sets of C_1 and C_2 can be divided into subsets of constrained inputs . Two subsets chosen from the two input sets are said to be constrained if any two input vectors chosen from each subset are constrained . The average constrained propagation probability will be the sum of the average propagation probabilities of the constrain subsets .

Definition 4

The transition probability matrix P for a sequential circuit is a square matrix whose entry p_{ij} is the probability of entering state j given that the present state is i .

Definition 5

A state-probability vector is said to be a stationary-state probability vector if $\Pi = \Pi P$. The π's are uniquely determined by the set of equations

$$\pi_i \geq 0 \ , \quad \sum_{\forall i} \pi_i = 1 \quad , \text{and} \quad \pi = \pi P$$

Now we will develop a model to aid us in the evaluation of the probability of detecting a failure , assuming that one exists , given m random input vectors . We will carry out our analysis for both Moore and Mealy machines .

A. Moore Type Sequential Circuits

Moore type sequential circuits can be represented by the structure shown in Figure 2 . Here we divide the sequential circuit into three parts . Part one is called the input circuit . It is a combinational circuit that generates the excitation signals for the memory elements . It has two sets of inputs . One set is X, the primary input lines . The other set is y, the state lines from the memory elements . The second part is the memory . This part consists of flip-flops . In this report we will consider memories consisting of D flip-flops . The input set Y to this part is the output of the input circuit . The third and final part is the output circuit which takes the state of the memory as an input and produces Z, the primary output .

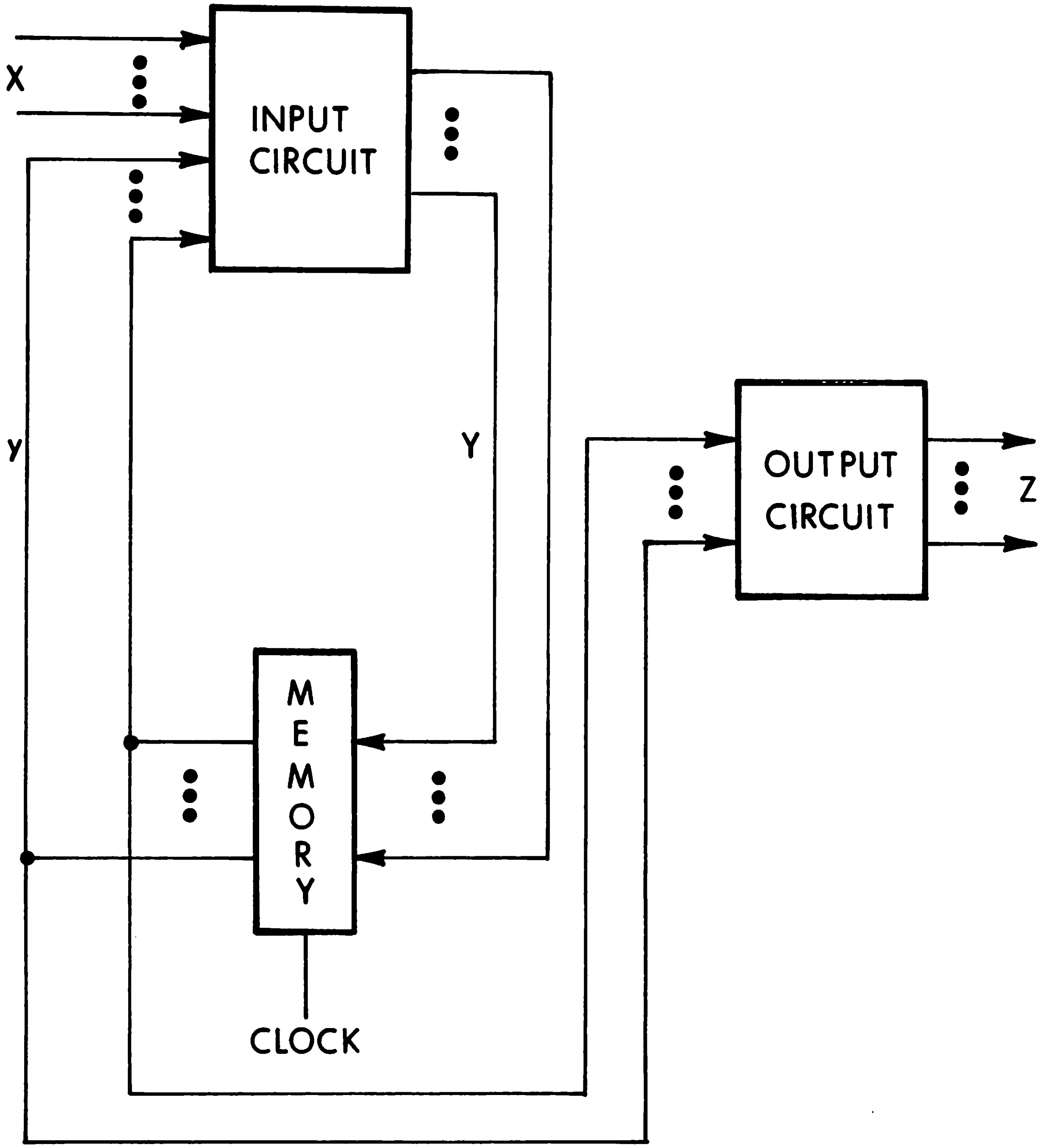

Fig. 2. Sequential circuit model (Moore Type)

The analysis presented will be based on the assumption that a hardware fault exists in any part, and its effect propagates to the primary output . There it can be compared with the output of the simulated circuit . The classical single stuck-at 0/1 fault model is assumed .

Faults can occur in the input circuit, memory or the output circuit . In this analysis we will consider each part failure separately . We will assume the existence of a fault in one of these parts.

The input circuit failure mode will include single stuck-at 0/1 on the primary input lines, its gate interconnection wires, and its output lines . A failure in the memory part will only cover single stuck-at 0/1 on its output lines . Finally the output circuit failure mode will include stuck-at 0/1 on the gate interconnection wires and the primary output lines .

The input vectors to the actual and the simulated input circuits are an example of a constrained input . The primary input lines represent the β lines in definition 2 . Let A be the constrained propagation probability for the input circuit .

The memory part can be modeled as a combinational circuit . For a fault free memory, the output will be equal to the input (after a certain delay) regardless of the state of the D flip-flop . Hence, the propagation probability of the memory can be evaluated using definition 1 . Let B be the propagation probability of the memory part .

Let C be the propagation probability for the output circuit . C can be evaluated using equation (1) .

Let q_1, q_2, and q_3 be the average probabilities of having an error at the output of the input, memory, and output circuits respectively due to the application of one input vector . Now we will analyze each part failure separately .

1. Input Circuit Failures

Faults in this circuit will effect the state excitation lines for the memory . This effect will change the single transition matrix P which in turn will change the stationary-state probability of the sequential circuit . Evaluating the stationary-state probabilities of the fualt free and the faulty circuits and having the primary input probabilities, we can obtain the probability distribution of the input sets for the actual (faulty) and fault free circuits . From these distributions we can evaluate A and q_1 . Using equation (1) we can evaluate B and C . From the stationary-state probabilities we can evaluate C . If the output of the input circuit is directly observable then the failure will be detected according to the value of q_1 . But since the only observable output is the one from the output circuit, then the error from the input circuit needs to propagate through the memory and the output circuit before it can be detected .

We define the following probabilities

P_n = Probability of the first detection starting from initial state, when the n'th input vector is applied, and

G_n = Probability of the first detection due to a feedback state which occured n time frames earlier, assuming that a new random input vector is applied at the begining of each time frame .

A feedback state is a situation where the good and the faulty circuits are in different states, and the resulting error does not propagate to the primary output . From Figure 3 we note that the probability of detecting a fault in the input circuit after the application of the first input vector is

$$P_1 = q_1 BC \qquad (2)$$

We define

$$G_1 = ABC \qquad (3)$$

For n greater than 1 we note that the probability of detection at the n'th input is equal to the sum of the following three mutually exclusive events :

1) No error is generated in the first input so detection occurs due to the next n-1 input vectors .

2) An error is generated by the first input but is blocked at the memory so detection occurs in the next n-1 input vectors .

3) An error is generated in the first input, and is propagated through the memory, but is blocked by the output circuit so it needs to repeat the propagation process during the next n-1 input vectors .

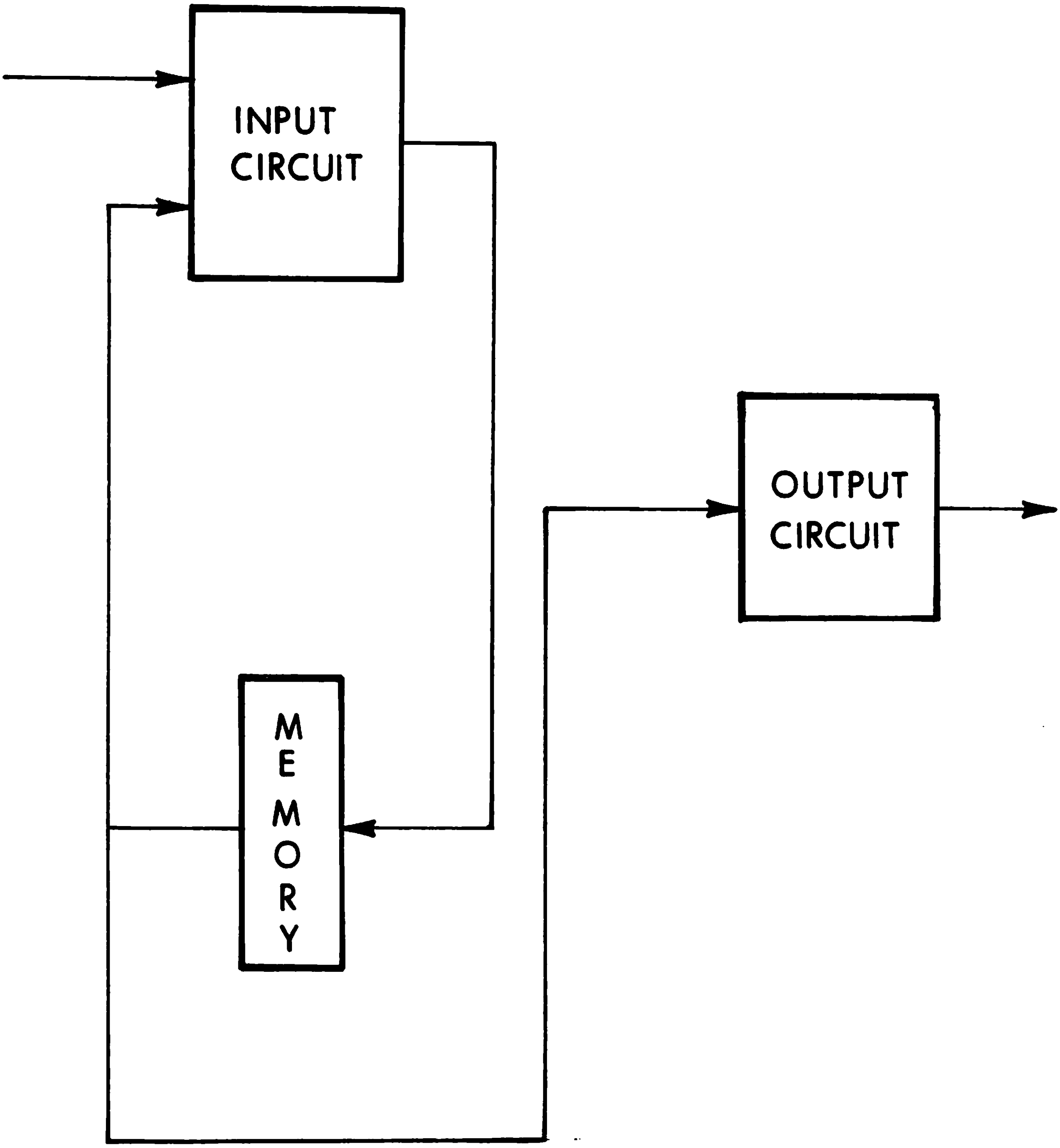

Fig. 3. Failure propagation path

Hence, we have

$$P_n = (1-q_1)P_{n-1} + q_1(1-B)P_{n-1} + q_1 B(1-C)G_{n-1} \qquad (4)$$

The feedback state at the n'th input is equal to the sum of three mutually exclusive events . They are

1) the error is blocked by the input circuit so detection occurs in the next n-1 input vectors,

2) the error propagates through the input circuit but is blocked by the memory so detection occurs in the next n-1 input vectors, and

3) the error propagate through the input circuit and the memory but is blocked by the output circuit so it needs be repeat the propagation process in the next n-1 inputs .

Hence, we have

$$G_n = (1-A)P_{n-1} + A(1-B)P_{n-1} + AB(1-C)G_{n-1} \qquad (5)$$

Equations (4) and (5) are two dependent difference equations . We can apply the z-transform method to solve for P as a function of n . We define

$$P(z) = \sum_{n=0}^{\infty} P_n z^n$$

and

$$G(z) = \sum_{n=0}^{\infty} G_n z^n$$

Now we multiply the P_n by z^n and sum over all applicable n . This yields

$$\sum_{n=2}^{\infty} P_n z^n = (1-q_1 B)\sum_{n=2}^{\infty} P_{n-1} z^n + q_1 B(1-C)\sum_{n=2}^{\infty} G_{n-1} z^n$$

$$\sum_{n=0}^{\infty} P_n z^n - zP_1 - P_0 = (1-q_1 B)z\left[\sum_{n=0}^{\infty} P_n z^n - P_0\right] + q_1 B(1-C)z\left[\sum_{n=0}^{\infty} G_n z^n - g_0\right]$$

Since $p_0 = g_0 = 0$, we have that

$$P(z) - zp_1 = (1-q_1 B)z\,P(z) + q_1 B\,(1-C)z\,G(z)$$

Rewriting we have

$$P(z)\left[1-(1-q_1 B)z\right] = zp_1 + q_1 B(1-C)z\,G(z) \qquad (6)$$

Applying the same procedure on equation (5) we obtain

$$G(z)\left[1 - AB(1-C)z\right] = zg_1 + (1-AB)z\,P(z)$$

Thus

$$G(z) = \frac{zg_1 + (1-AB)z\,P(z)}{1 - AB(1-C)z}$$

Substituting the value of G(z) in equation (6) we find

$$P(z)\left[1-(1-q_1 B)z\right] = zP_1 + \frac{q_1 B(1-C)g_1 z^2 + q_1 B(1-C)(1-AB)z^2\,P(z)}{1 - AB(1-C)z}$$

$$P(z)\left[1-(1-q_1 B)z - \frac{q_1 B(1-C)(1-AB)z^2}{1-AB(1-C)z}\right] = zP_1 + \frac{q_1 B(1-C)g_1\,z^2}{1-AB(1-C)z}$$

Using equations (2) and (3) we have

$$P(z)\left[\frac{1-\big(AB(1-C)+(1-q_1 B)\big)z + (1-C)(AB-q_1 B)z^2}{1-AB(1-C)z}\right] = \frac{q_1 BC\,z}{1-AB(1-C)z}$$

Since C is greater than zero then we have

$$P(z) = \frac{q_1 BC\,z}{1 - bz + az^2}$$

where

$$a = (1-C)(AB - q_1 B)\ , \text{ and}$$
$$b = 1 - q_1 B + AB(1-C)$$

Factoring the denominator we obtain

$$P(z) = \frac{q_1 BC z}{(1-\alpha_1 z)(1-\alpha_2 Z)}$$

where $1/\alpha_1$ and $1/\alpha_2$ are solutions of the quadratic equation in the denominator . Using partial-fraction expansion of this last form we obtain

$$P(z) = \frac{A_1}{(1-\alpha_1 z)} + \frac{A_2}{(1-\alpha_2 z)}$$

where

$$A_1 = \frac{q_1 BC}{\alpha_1 - \alpha_2}$$

and

$$A_2 = \frac{q_1 BC}{\alpha_2 - \alpha_1}$$

which can be inverted to give the final solution

$$P(n) = A_1 (\alpha_1)^n + A_2 (\alpha_2)^n \qquad n = 1, 2, 3, \ldots \qquad (7)$$

Note that A_1, α_1, A_2, and α_2 are constants which can be obtained from the values of A, B, C, and q_1.

2. Failures in The Memory Elements

The most general assumption we can make concerning faults in the memory is that one of the flip-flops has a stuck-at fault at its output . This kind of fault will block up to half of the states of the memory . We note that each memory fault modifies the transition matrix P . Hence, we need to evaluate the stationary-state probability for the modified circuit . Having the primary input lines probabilities and the stationary-state probabilities we can evaluate the probability distributions of the input sets for the memory of the actual and the simulated circuits . From these distributions we can evaluate B and q_2. A and C can be evaluated in a similar manner as previously explained .

If the internal state of the memory is directly observable then the fault will be detected with probability q_2 after the application of one input vector . Since the only observable states are the initial and final ones , then an error in the memory output needs to propagate through the output circuit so that it can be detected . The probability of detecting an existing fault in the memory as a result of applying the first input vector is

$$P_1 = q_2 C \qquad (8)$$

The value of B_1 is the same as in equation (3) . From Figure 3 we can deduce that the probability of detection at the n'th input is the sum of two mutually exclusive events . They are (1) no error is generated by the first input vector so detection occurs due to the next n-1 input vectors and (2) an error is generated by the first input but is masked by the output circuit so it needs to repropagate through the circuit during the next n-1 input vectors . Hence, we have

$$P_n = (1-q_2)P_{n-1} + q_2(1-C)G_{n-1} \qquad (9)$$

G_n is the same as in equation (5) . Equations (9) and (5) are a system of difference equations which can be solved using the z-transform method . Following the same procedure as in the solution of the input circuit difference equations we find that

$$P(z)\left[\frac{1-(AB(1-C)+(1-q_2))z+(1-C)(AB-q_2)z^2}{1-AB(1-C)z}\right] = \frac{q_2 C z}{1-AB(1-C)z}$$

Since C is greater than zero, canceling the denominators we obtain

$$P(z) = \frac{q_2 C z}{1-bz+az^2}$$

where

$$a = (1-C)(AB-q_2)\text{ , and}$$
$$b = 1-q_2+AB(1-C)$$

Using partial-fraction expansion and inverting we have

$$P(n) = B_1(\beta_1)^n + B_2(\beta_2)^n \qquad n=1,2,3,\cdots \qquad (10)$$

where

$$B_1 = \frac{q_2 C}{\beta_1-\beta_2}\text{ , and } B_2 = \frac{q_2 C}{\beta_2-\beta_1}$$

$1/\beta_1$ and $1/\beta_2$ are solutions of the quadratic equation in the denominator of P(z) .

3. Failures in the Output Circuit

A nonredundant fault in this circuit can be detected with probability q_3 after the application of the first input vector . q_3 can be evaluated from the input set probability distribution for the output circuit which is equal to the stationary-state probability . Since the output of this circuit is a primary output then error propagation is not needed . The probability of detecting a fault in the output circuit after the application of the first input vector is

$$P_1 = q_3 \qquad (11)$$

So the probability of detecting a fault at the n'th input vector is

$$\begin{aligned} P_n &= (1-q_3)P_{n-1} \\ &= (1-q_3)(1-q_3)\ldots \; P_1 \\ &= (1-q_3)^{n-1} q_3 \qquad (12) \end{aligned}$$

The probability of detecting a fault in n or less input vectors is

$$\begin{aligned} PD &= \sum_{i=1}^{n} P_i \\ &= 1-(1-q_3)^n \qquad (13) \end{aligned}$$

Let PI(m) , PM(m) , and PO(m) be the probability of detecting a fault in the input circuit, memory , or output circuit, respectively using a test of length m . If we assume that only one part of the sequential circuit is faulty, then we can calculate the probability of detecting a single fault in the entire circuit . Let P_i , P_m , and P_o be the probability that the faulty part is the input circuit, memory or output circuit respectively . Thus we have that the probability of detecting a fault in the circuit, assuming that one exists, for a test of length m is

$$PD(m) = P_i PI(m) + P_m PM(m) + P_o PO(m) \qquad (14)$$

Note that P_i , P_m , and P_o could be estimated as a function of either the number of wires , number of gates , or the size of their associated part in the circuit .

Another source of detection can be achieved (if available) by comparing the final state of the actual machine with the final state of the simulated one . Note that such detection is only for faults in the input circuit and the memory .

Let P_n be the probability of having different states in the good and the faulty circuits, when the n'th input is applied . Let G_n be the probability of having different states due to a feedback state which occurred n time frames earlier . A feedback state in this case is a situation where the good and the faulty circuits are in different states, but no final state dump occurs .

If we assume that the fault is in the input circuit then the probability that the state of the actual machine is different than the state of the simulated one, after the application of one input vector is

$$P_1 = q_1 B \qquad (15)$$

We let

$$G_1 = AB \qquad (16)$$

P_n is equal to the sum of three mutually exclusive events . They are

1) no error is generated at the output of the input circuit due to the application of the first input so the difference in the states is due to the next n-1 input vectors,

2) an error is generated at the output of the input circuit due to the application of the first input vector but is blocked by the memory so the difference in the state is due to the next n-1 inputs, and

3) an error is generated at the output of the input circuit and it produces a different state but no dump of state occurs so it needs to propagate through the input circuit and the memory for the remaining n-1 inputs .

Hence, we have

$$P_n = (1-q_1)P_{n-1} + q_1(1-B)P_{n-1} + q_1 BG_{n-1} \tag{17}$$

G_n is also the sum of three mutually exclusive events . They are

1) the error is blocked by the input circuit so the difference in states is due to the next n-1 input vectors,

2) the error is propagated through the input circuit but is blocked by the memory so the difference in states is due to the next n-1 input vectors, and

3) the error is propagated through the input circuit and the memory but no state dump occurs so it needed to repropagate during the next n-1 input vectors .

Hence, we have

$$G_n = (1-A)P_{n-1} + A(1-B)P_{n-1} + ABG_{n-1} \tag{18}$$

This system of difference equations can be solved, using the z-transform, to obtain the equilibrium probability of having a different state in the actual and simulated circuits . Multiplying equation (17) by z and summing over all applicable n, we have

$$\sum_{n=2}^{\infty} P_n z^n = (1-q_1 B)\sum_{n=2}^{\infty} P_{n-2} z^n + q_1 B \sum_{n=2}^{\infty} G_{n-1} z^n$$

Following a similar procedure, as in the solution of the input circuit difference equations, we obtain

$$P(z) = \frac{z\, q_1 B}{1-(1+AB-q_1 B)z+(AB-q_1 B)z^2}$$

Using the final value theorem of the z-transform we have

$$\lim_{z\to 1} (1-z)\, P(z) = P_\infty$$

Hence,

$$P_\infty = \lim_{z\to 1} \frac{z q_1 B - z^2 q_1 B}{1 - (1 + AB - q_1 B)z + (AB - q_1 B)z^2}$$

Direct application yields the indeterminate form 0/0 so we must use L'Hospital rule, which gives us

$$P_\infty = \frac{q_1 B}{1 - AB + q_1 B} \qquad (19)$$

If the failure is in the memory then the probability of detection, i.e. having different states for the actual and simulated circuit, after the application of the first input vector is

$$P_1 = q_2 \qquad (20)$$

Again we let

$$G_1 = AB \qquad (21)$$

The probability of having different states at the n'th input is the sum of two mutually exclusive events . They are

1) no error occurs due to the first input to the memory so the difference in the states occurs in the next n-1 input vectors, and

2) an error is generated due to the application of the first input vector but no dump of the state occurs so it needs to repropagate during the next n-1 input vectors .

Hence, we have

$$P_n = (1-q_2)P_{n-1} + q_2 G_{n-1} \qquad (22)$$

where G_{n-1} is the same as in equation (18) . The system of difference equations can again be solved using z-transform method to find the equilibrium probability of having different state .

Following a similar procedure as in the solution of the input circuit difference equations we obtain

$$P(z) = \frac{z\,q_{b2}}{1-(1+AB-q_{b2})z+(AB-q_{b2})\,z^2}$$

Using the final value theorem of the z-transform we have

$$P_\infty = \lim_{z\to 1} \frac{zq_{b2}-q_{2}z^2}{1-(1+AB-q_{b2})z+(AB-q_{b2})z^2}$$

Applying L'Hospital's rule we obtain

$$P_\infty = \frac{q_{b2}}{1-AB+q_{b2}}$$

Now if the fault is either in the input circuit or in the memory , then we may have two sources of detection . One source is obtained by comparing the outputs, and the other is obtained by comparing the final states of the actual and simulated circuits . The two detection sources can be added to the probability of detection of the entire circuit . Hence, we obtain

$$PD = P_i\,(PI_1 + PI_2 - PI_1\,PI_2) + P_m\,(PM_1 + PM_2 - PM_1\,PM_2) + P_o\,PO \qquad (24)$$

where PI_1 (PM_1) and PI_2 (PM_2) are the first and the second detection sources for the input circuit (memory) respectively .

B. A Note on Mealy Machines

Figure 4 shows a general model for a Mealy type synchronous sequential machine . We note that the only difference between this Figure and Figure 2 is the input to the output circuit .

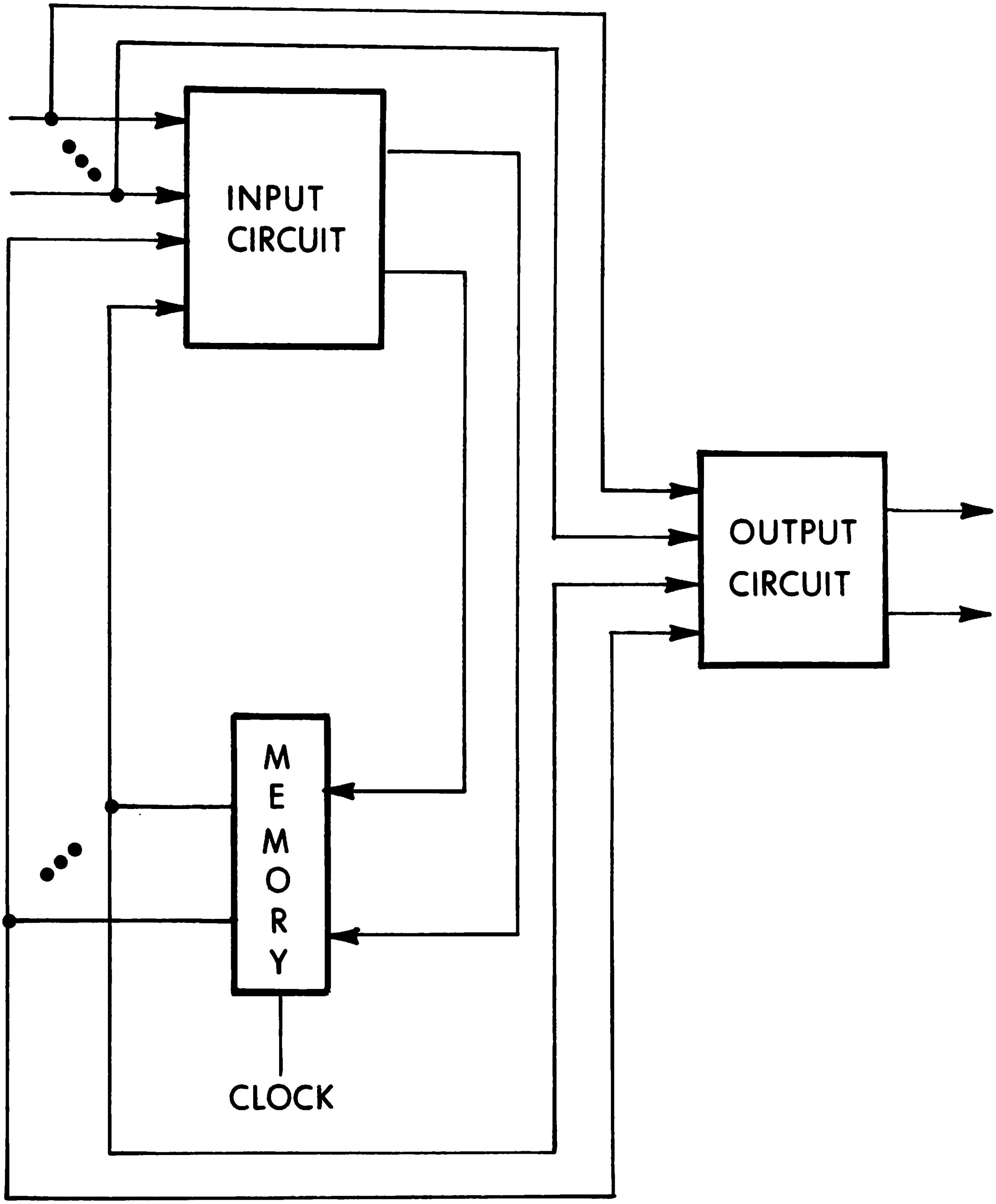

Fig. 4. Mealy type sequential circuit model

The input sets to the actual and simulated circuits are constrained . Thus the only change in this model will be in the values of $\underline{q}_3$ and C . Hence,the same equations we obtained for the Moore model can be applied to the Mealy model .

III. Example

We will illustrate the material presented on the sequential circuit given in Figure 5 . Let the probability of having a 1 on a primary input line be 0.6 . Figure 6 shows a state-transition diagram of the sequential circuit . From the diagram we have

$$P = \begin{bmatrix} 0.4 & 0.0 & 0.6 & 0.0 \\ 0.0 & 0.0 & 0.0 & 1.0 \\ 0.4 & 0.6 & 0.0 & 0.0 \\ 0.6 & 0.4 & 0.0 & 0.0 \end{bmatrix}$$

Solving the equation $\pi = \pi P$ we obtain

$$\pi_{00} = 0.4\ \pi_{00} + 0.4\ \pi_{10} + 0.6\ \pi_{11}$$
$$\pi_{01} = 0.6\ \pi_{10} + 0.4\ \pi_{11}$$
$$\pi_{10} = 0.6\ \pi_{00}$$
$$\pi_{11} = \pi_{01}$$

In order to solve this system of equations we need one more equation that is

$$1 = \pi_{00} + \pi_{01} + \pi_{10} + \pi_{11}$$

Solving we obtain

$$\pi_{00} = 0.3571$$
$$\pi_{01} = \pi_{10} = \pi_{11} = 0.2143$$

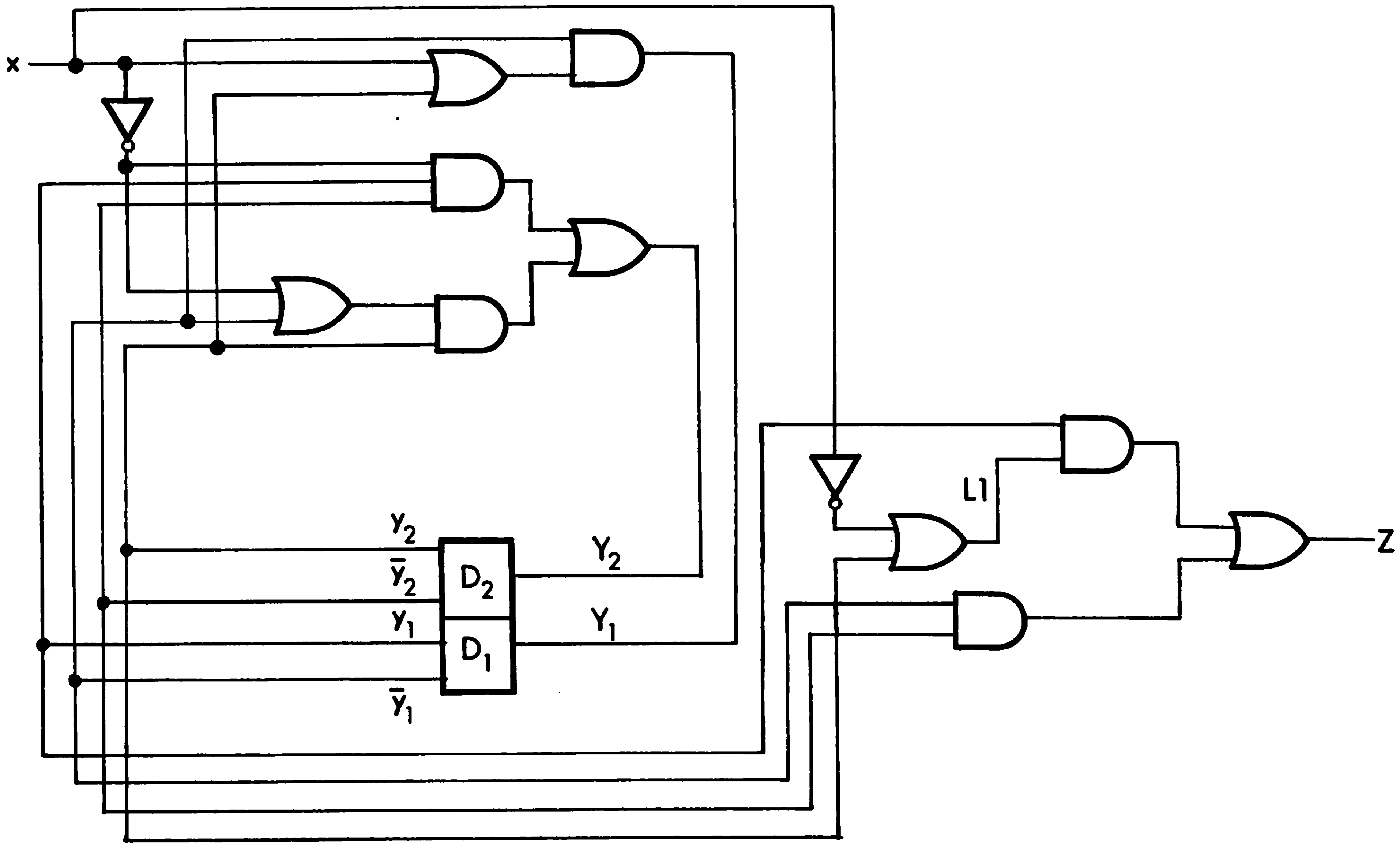

Fig. 5. Circuit diagram

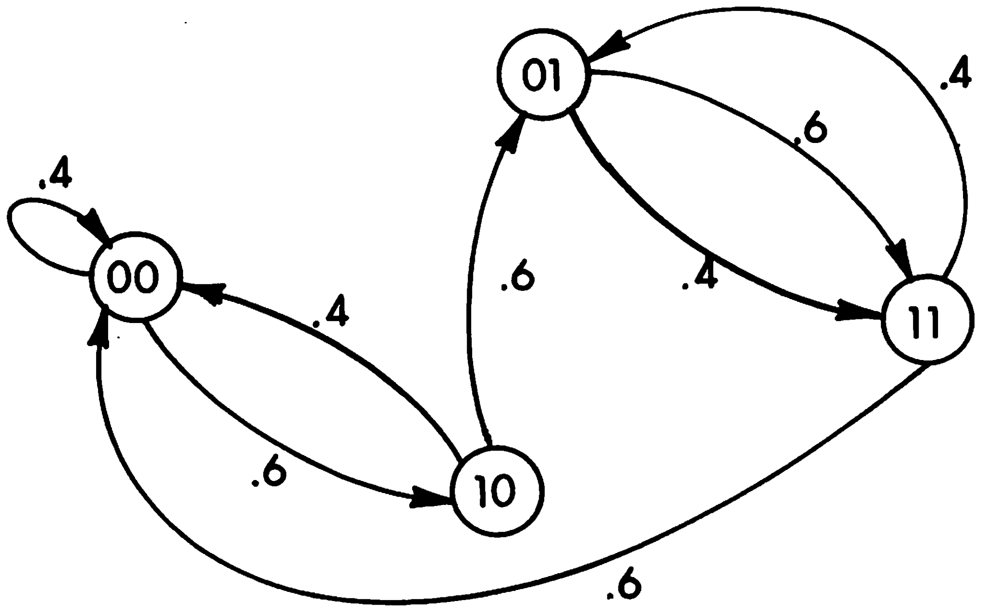

Fig. 6. State-transition diagram for the fault free circuit shown in Figure 5

This gives us the stationary-state probabilities . Let us consider the fault Y_1 s-a-1 . Figure 7 shows the state-transition diagram of the faulty sequential circuit . From the diagram we find the new transition probability matrix to be

$$P = \begin{bmatrix} 0.0 & 0.0 & 1.0 & 0.0 \\ 0.0 & 0.0 & 0.0 & 1.0 \\ 0.0 & 0.0 & 0.4 & 0.6 \\ 0.0 & 0.0 & 0.6 & 0.4 \end{bmatrix}$$

Solving for the stationary-state distribution vector we have

$$\pi_{00} = \pi_{01} = 0.0$$

$$\pi_{10} = \pi_{11} = 0.5$$

Tables 1 and 2 show the truth table of the input circuit for fault free and faulty circuits respectively . From table 2 we note that any input vector is a test vector . Hence, $q_1 = 1$. From definition 3 we obtain A = 0.7292 .

Since any two different inputs to the memory will produce a different output then B = 1 .

Tables 3 and 4 show the truth table for the output circuit of the fault free and faulty circuits respectively . The input to the fault free and faulty circuits is constrained . Hence, from definition 3 we obtain C = 0.4376

Since the fault is in the input circuit then equation (7) can be used to evaluate the probability of detection . Figure 8 shows

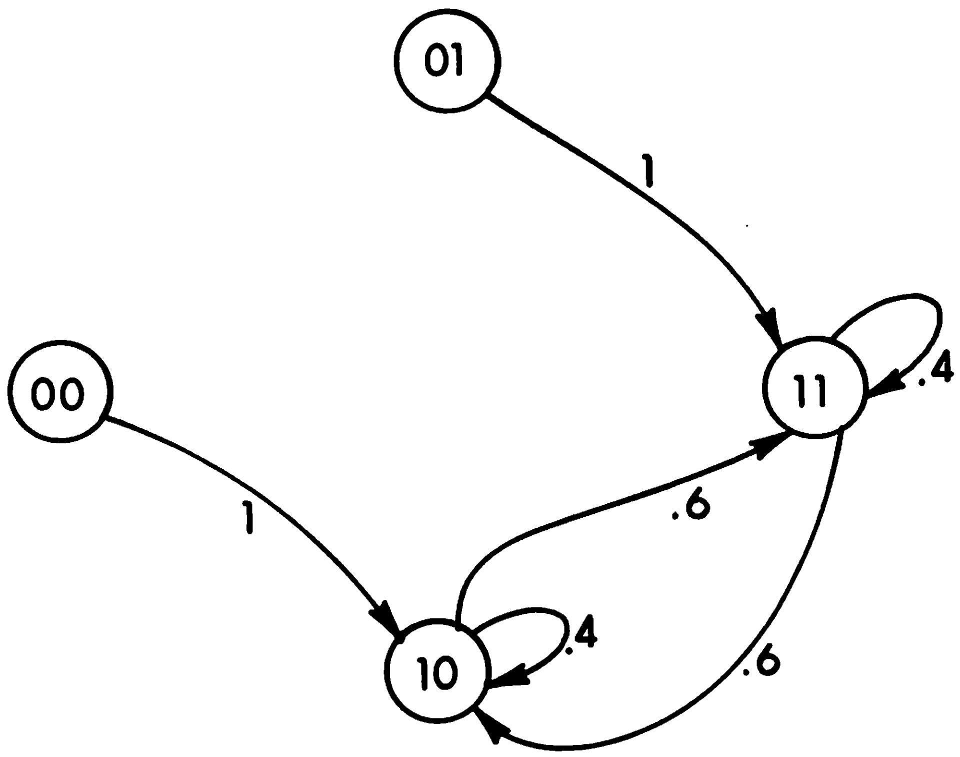

Fig. 7. State-transition diagram for the faulty circuit

Table 1. Fault free input circuit truth table

x	y_1	y_2	$\bar{y}_1$	$\bar{y}_2$	Y_1	Y_2
0	0	0	1	1	0	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	1	0	0	0	1
1	0	0	1	1	1	0
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	1	0	0	0	0

Table 2. Faulty input circuit truth table

x	y_1	y_2	$\bar{y}_1$	$\bar{y}_2$	Y_1	Y_2
0	1	0	0	1	1	0
0	1	1	0	0	1	1
1	1	0	0	1	1	1
1	1	1	0	0	1	0

Table 3. Fault free output circuit truth table

x	y_1	y_2	$\bar{y}_1$	$\bar{y}_2$	Z
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	0	0

Table 4. Faulty output circuit truth table

x	y_1	y_2	$\bar{y}_1$	$\bar{y}_2$	Z
0	1	0	0	1	1
0	1	1	0	0	1
1	1	0	0	1	1
1	1	1	0	0	0

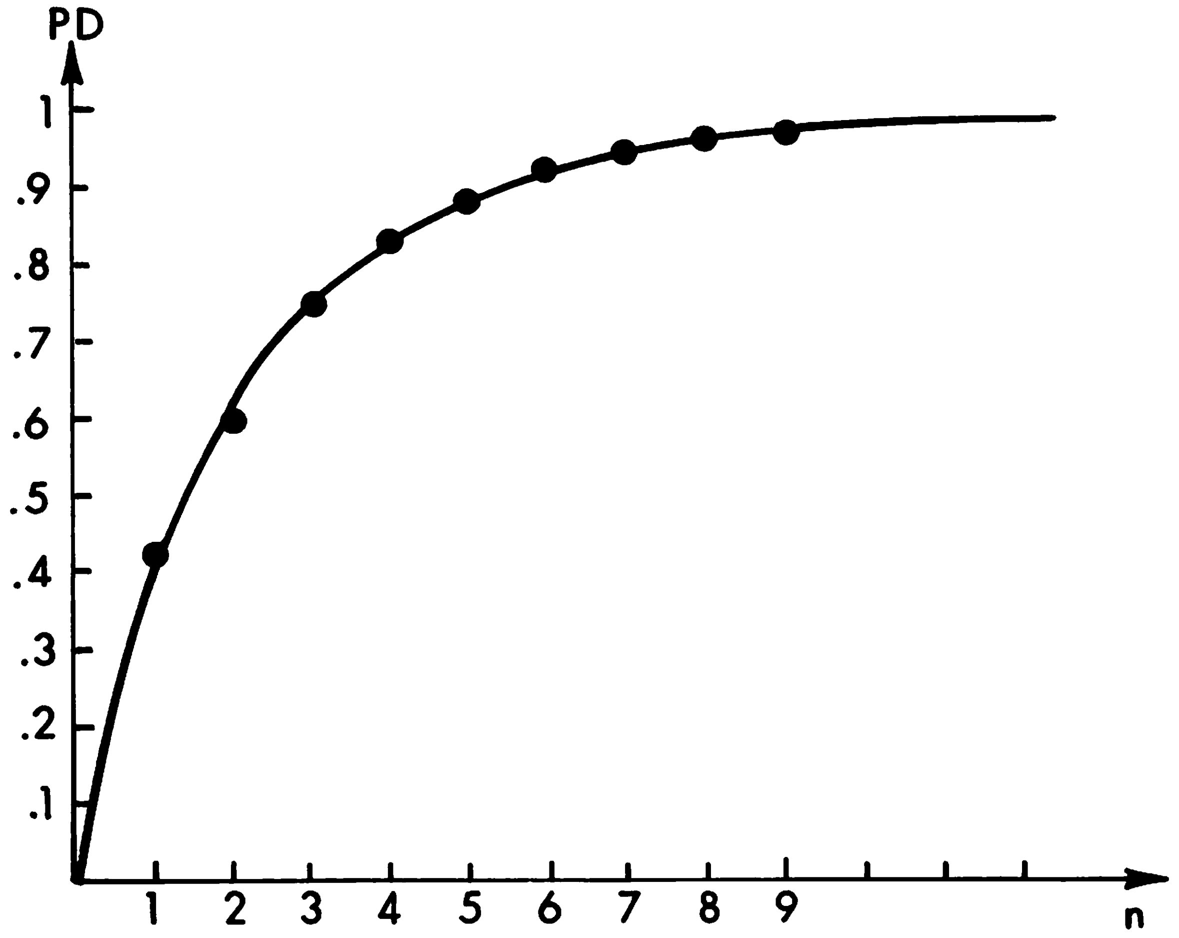

Fig. 8. The probability of detection vs. the number of random input vectors for the fault Y_1 s-a-1

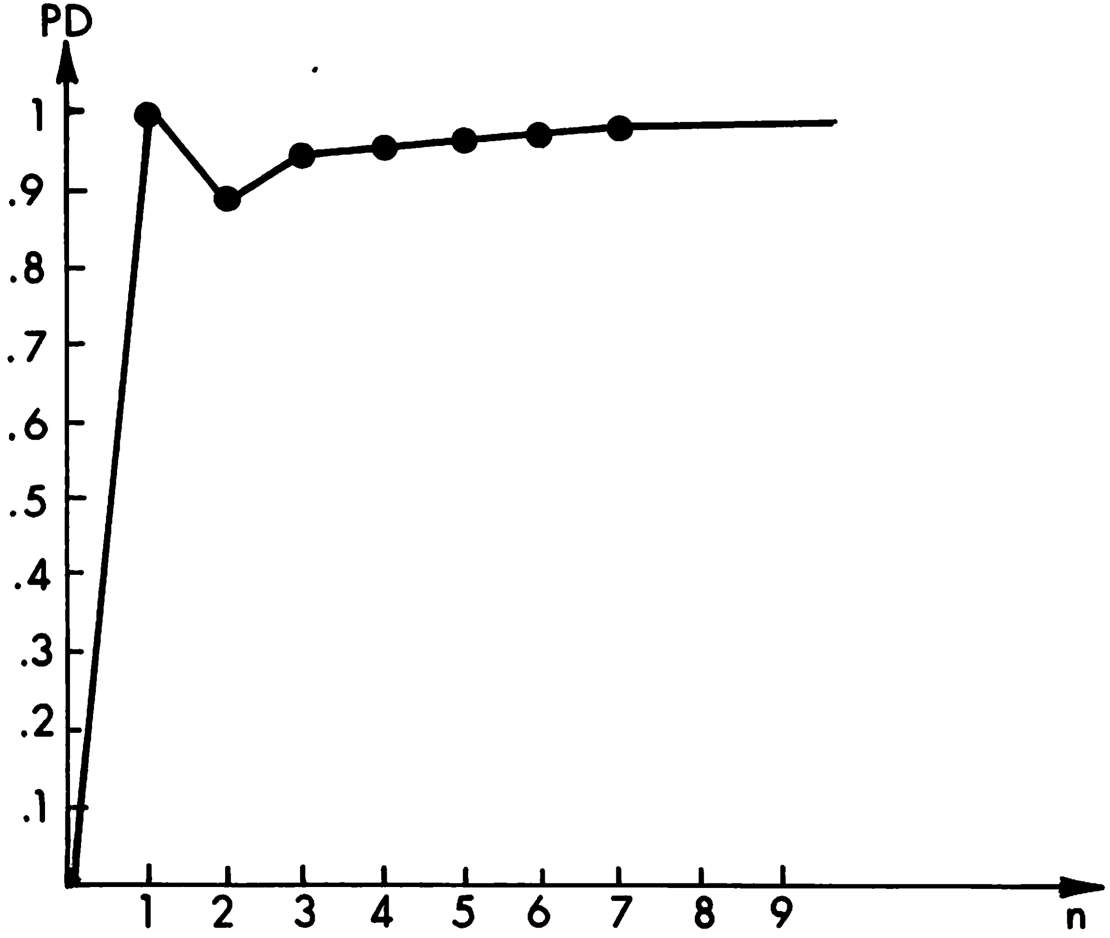

Fig. 9. The total probability of detection vs. the number of random input vectors for the fault Y_1 s-a-1

PD as a function of the number of input vectors . Figure 9 shows the total PD where we include both sources of detection as a function of the number of input vector .

Now we will consider the fault y_1 s-a-1 . The state-transition diagram of the faulty circuits is the same as the one for the fault Y_1 s-a-1 . So the stationary-state distributions are

$$\pi_{00} = \pi_{01} = 0.0$$

$$\pi_{10} = \pi_{11} = 0.5$$

Note that this fault has the same effect on the stationary-state probability vector of the circuit but it modifies the values of A and B . Tables 5 and 6 show the truth table of the memory for the fault free and faulty circuits respectively . From Table 6 we obtain $q_2 = 1$. From equation (1) we obtain B = 0.7 . Table 7 shows the truth table of the input circuit for the faulty machine . The value of A is obtained from definition 3 . Solving we obtain A = 0.9099 . Since we have the same input probability distribution for the output circuit as we have for the previous fault then C = 0.4376 . Since this fault is considered as a memory fault then equation (10) can be used to obtain PD . Figure 10 shows PD as a function of the number of input vectors.

Finally we will consider a fault in the output circuit . Let L1 be s-a-0 . From table 3 we find that inputs 011 and 110 detect the fault . Hence, $q_3 = 0.2143$ Figure 11 shows PD as a function of the number of input vectors .

Table 5. The fault free memory truth table

Y_1	Y_2	y_1	y_2
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Table 6. The faulty memory truth table

Y_1	Y_2	y_1	y_2
0	0	1	0
0	1	1	1

Table 7. The faulty input circuit truth table

x	y_1	y_2	$\bar{y}_1$	$\bar{y}_2$	Y_1	Y_2
0	1	0	0	1	0	0
0	1	1	0	0	0	1
1	1	0	0	1	0	1
1	1	1	0	0	0	0

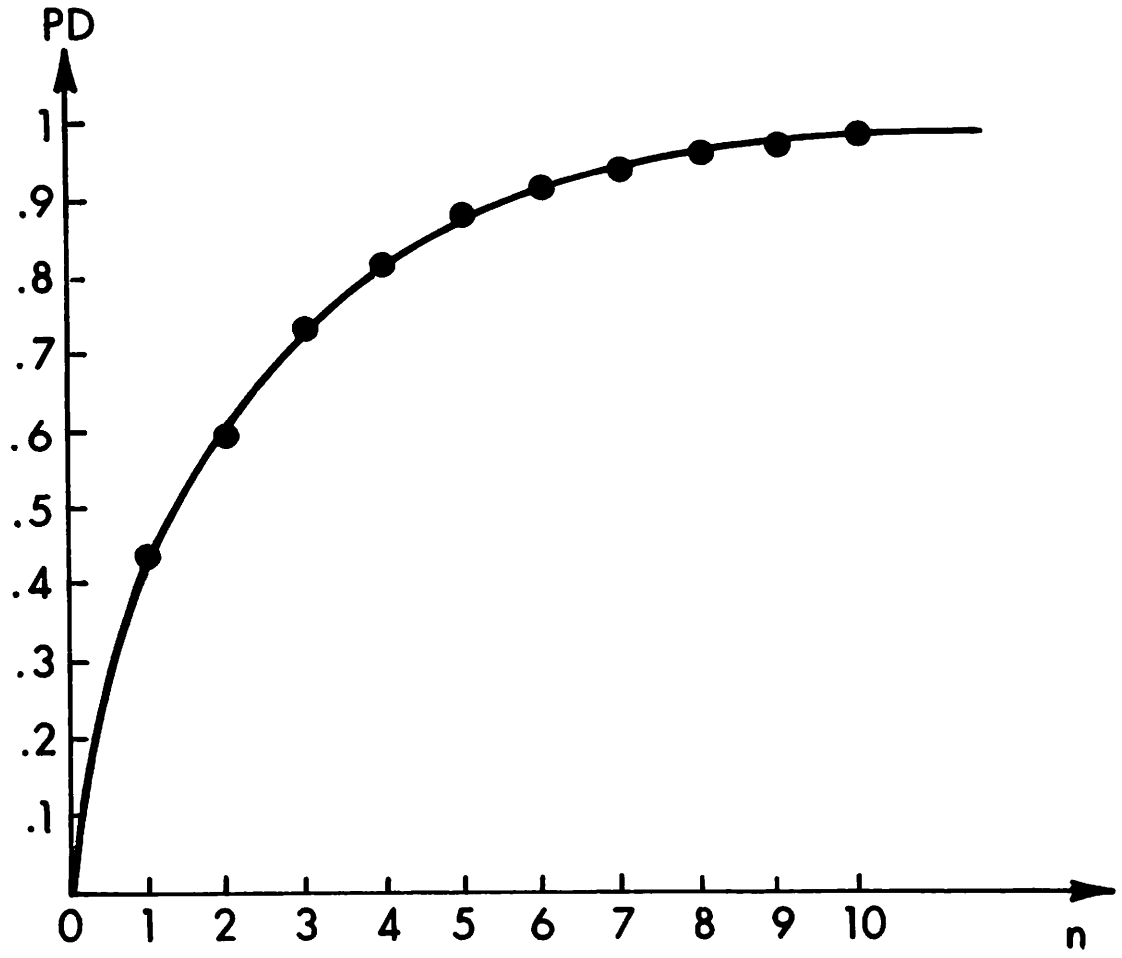

Fig. 10. PD vs. n for the memory fault y_1 s-a-1

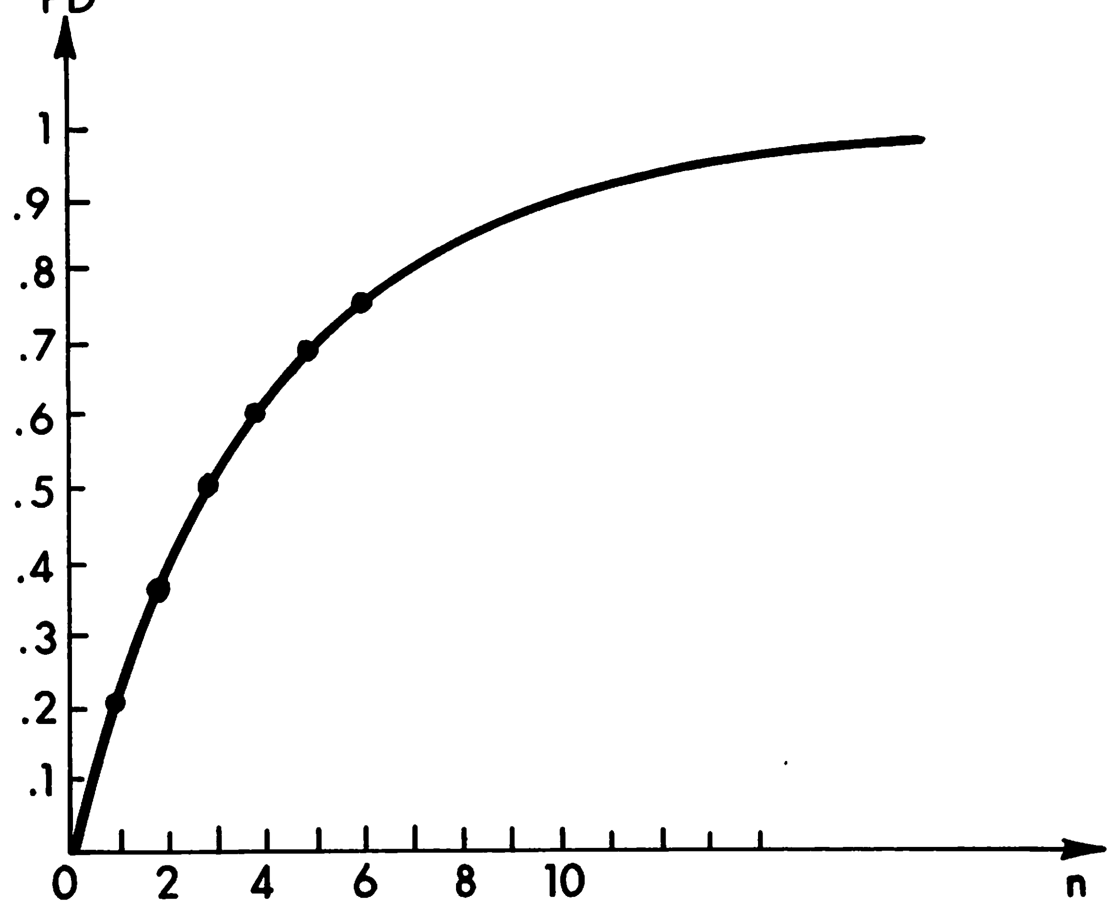

Fig. 11. PD vs. n for an output circuit fault

Conclusion

We have presented a method to calculate the probability of detecting a single stuck-at fault in a sequential circuit . This method separate then considers each part of the sequential circuit separately . This method has been applied to a simple sequential circuit .

The method presented is needed to compute the parameter PD . This parameter is used in the roving emulation performance analysis . We note that complex calculations are required to obtain circuit parameters . This complexity grows rapidly with the circuit size . This leads us to partition large circuits into smaller feasible combinational and sequential circuits .

Figure 8 specifies a test of 6 inputs to have probability 0.9 of testing the fault, while Figure 9 specifies 2 inputs when the second detection source (final state comparison) is added .

The average detection probability for the entire circuit can be obtained by finding an average value for each parameter over a prescribed set of faults for each part of the sequential circuit model .

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