

Wiring Space Estimation¹ of Master Slice ICS

**Technical Report CRI-85-30
(DISC 83-5 - June 1983)**

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¹This research was supported by Army Research Office Grant DAAG29-80-K-0083.

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Wiring Space Estimation of Master Slice ICS		5. TYPE OF REPORT & PERIOD COVERED Technical 1/85 ~ 8/83
		6. PERFORMING ORG. REPORT NUMBER DISC / 83-5
7. AUTHOR(s) Sarma Sastry		8. CONTRACT OR GRANT NUMBER(s) DAAG29-80-K-0083
9. PERFORMING ORGANIZATION NAME AND ADDRESS Department of Electrical Engineering - Systems University of Southern California Los Angeles, CA 90089-0781		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS U. S. Army Research Office Post Office Box 12211 Research Triangle Park, NC 27709		12. REPORT DATE June 1983
		13. NUMBER OF PAGES 34
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) NA		
18. SUPPLEMENTARY NOTES The view, opinions, and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) wireability, wiring space estimation, routing channels, channel-width estimation, master-slice, gate array, integrated circuit, rent's rule, design automation area estimation		
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ABSTRACT

In this report we present a stochastic model for estimating the amount of wiring space (i.e. the dimensions of the routing channels) needed for a master-slice integrated circuit. A master-slice IC is modelled as an $N \times N$ lattice of points, with each point representing the intersection of a horizontal and vertical channel. Wires are assumed to follow minimal rectilinear paths and allowed to use as many vias as necessary. Wires at an intersection are classified as belonging to one of six classes. Distributions of the number of each type at a channel intersection are derived. As the dimensions of a channel intersection are functions of the number of wires belonging to each class, expected values of these quantities are derived. The problem of making estimates sensitive to placement strategy is discussed. In particular, the intimate relation between placement, Rent's Rule and wire length distribution is addressed. Finally, preliminary results on extending the model to allow wires with only a fixed number of vias are presented.

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1 Background

An integrated circuit (IC) realizing a function f consists of a large collection of sequential and combinational subcircuits, each realizing a subfunction f_i , which, when interconnected by wires realize the composite function f . The process of IC design is essentially one of mapping a graph representation of f , where the nodes represent subcircuits and the edges represent interconnections, onto a planar surface. This transformation generally consists of the following steps:

1. Selection of a set of components that correspond to the nodes of the graph.
2. Assigning physical locations to the components on the planar surface. This is known as the placement problem.
3. Interconnecting the placed circuits by wires, with the wires between the circuits corresponding to the edges between nodes in the logic graph. This is known as the routing problem.

The quality of the placement and routing is measured by various parameters, the two more common ones being area of the resulting IC and the average wire length. Other parameters such as propagation delay through wires and power consumption have not been dealt with explicitly, and it is generally agreed that wire length encompasses these two parameters.

With regard to area and wire length, placement and routing are mutually competing tasks. That is, placement must be done before routing the wires. However, to obtain the optimal placement with respect to area and wire length, knowledge about the routes of the wires is needed. In addition to this problem of minimizing area and wire length, fabrication technology imposes certain design constraints such as minimal separation between wires, minimal sizes of transistors, etc., which have to be satisfied by the optimal placement and routing configurations. Recently, it has been shown [18] that the problem of compacting an IC layout subject to these constraints belongs to the class of NP-complete problems. This coupled with the fact that the state-of-art of

fabrication technology makes it possible to design ICs having almost a million devices forces the designers to seek good sub-optimal solutions that can be obtained rapidly.

The various design styles currently in practice reflect this desire to shorten the design cycle time. In general, there are three basic design styles, which are listed below in increasing order of design effort.

1. Master Slice (also called Gate Array)
2. Poly Cell
3. Custom

1.1 Master Slice Design

Master Slice (MS) or Gate Array design is currently the most popular method of IC design in industry. Briefly, a MS chip consists of a two-dimensional array of uniformly spaced logic cells of identical size that have been pre-fabricated up to the diffusion layer. Each logic cell consists of a few uncommitted transistors and resistors which, when interconnected in various ways will realize some simple Boolean function such as a logic gate or a latch. Placement of logic consists of assigning the circuits to one or more of these basic cells. Once a circuit is assigned to a cell the transistors are interconnected in such a way as to realize the function of the circuit. The spaces between cells, called channels, are used to route the wires connecting the cells. Each channel has a number of tracks in which the wires lie. In MS designs the number of tracks in a channel, i.e., the width of the channel, is constant. Once the placement is complete the wire routing phase begins and consists of two phases.

The first phase, called Global wiring or Loose wiring [11] simply assigns wires to channels, assuming connections are made from the center of the cells. Each channel has pre-defined capacity, i.e., has allocated to it a given

number of tracks, which may not be exceeded. Wires follow rectilinear paths with horizontal wire segments on one plane and vertical segments on another plane. Wires change direction, i.e., switch planes, by the use of vias, which are holes that provide contact between the two planes. The maximum number of vias allowed at an intersection of a horizontal and vertical channel is fixed and may not be exceeded. When the number of wires allocated to a channel during this phase exceeds the channel capacity a Global Overflow is said to occur. The output of the Global Wiring phase is a list channels assigned to each wire and the locations of the global overflows.

The second phase, called the Exact Embedding phase, assigns wires to specific tracks within a channel. Usually, all vertical wire segments are allocated tracks first, followed by a horizontal track assignment. When a connection cannot be completed at this phase an Actual Overflow is said to occur.

The more sophisticated Global Wiring programs attempt to smooth out differences between the channel supply and demand values while reducing the number of global overflows. The success of the exact embedding phase depends on the quality of the global wiring phase, however, having no global overflows does not guarantee that 100% wiring completion can be achieved. In general, after an initial run of the two phases, channel capacities are modified by the user to reduce the number of overflows and the routing steps repeated. When the number of actual overflows is sufficiently small the remaining incomplete connections are manually completed.

1.2 Advantages and Disadvantages of MS Design

The regularity of MS structures provides for a number of advantages over other design styles, a reason for their great success in industry. These are

1. It provides for relatively short design cycle times.

2. It is very cost effective for low volume designs where tolerance limits on power and timing are not too critical.
3. The placement and routing phases have been automated to a large degree

The price paid for having identical cells and uniform routing channels is

1. It is difficult to adjust path delays as all transistors are of fixed size. This implies that the chip would operate much slower.
2. As arrays are pre-fabricated up to the interconnect stage, the exact access points within a cell are not known. Thus more than necessary contact points have to be provided with the resulting chip being larger than necessary.
3. Chips have relatively low density.

1.3 PolyCell Design

PolyCell design offers one additional degree of freedom over MS design. In PolyCell design the height of a row of cells is uniform, however, different rows may have different heights and this variation is usually in multiples of some unit. This allows the designer to use functional blocks, e.g. ALUs, Registers, etc., which have been custom designed and pre-defined in a library. Once the library modules have been selected, they are placed in rows and interconnected. Unlike MS designs, the channel widths are not fixed and during routing, tracks are added according to demand to ensure 100% routing completion.

The PolyCell design style enjoys a number of advantages over MS designs.

These are

1. Individual functional units can be fine tuned to consume less power and operate faster.
2. Chips are smaller as it is no longer necessary to provide extra access points for cells. In addition components can be made to abutt horizontally, decreasing the amount of wiring.
3. Very high device utilization can be achieved.

4. 100% routing completion can be achieved as the tracks are allocated to channels according to demand.

1.4 Custom Design

Custom design is the next logical step from poly-cells. Here an additional degree of freedom is given to the designer allowing components to be of arbitrary size and shape. Custom tailoring the components according to the designer's needs has the obvious advantages of faster circuits, higher component density, smaller area, etc. In fact, since VLSI provides for the possibility of very high component density, custom design has become the main focus of research. The principal problem faced by designers of custom circuits is that the solution space of the placement and routing problems is prohibitively large. In addition, as no pre-fabrication up to any level is done, the entire set of processing steps has to be carried out at each iteration. Thus custom design without any restrictions to the structure results in prohibitively long design cycle times. Currently, it is cost effective only for small, special purpose, high volume designs.

1.5 Motivation

Recognizing that in all these design styles the solution space for the placement and routing problems is exponential in nature, the search for optimal solutions is, in practice, not possible. It seems natural then to ask how one could obtain estimates of the measures used for assessing the quality of the solutions a priori. This would enable designers to eliminate many of the feasible points of the solution space before actually carrying out the algorithms.

As mentioned earlier, area and wire length have been the two most common measures of placement and routing. It has long been recognized that the space consumed by wiring is a very significant factor in determining the area of the IC. Therefore in assessing a given placement, the question as to how much

wiring space is needed is crucial. This estimate, if too large, can be used to select another placement and the process repeated. Once the designer is satisfied with the estimate of the wiring space for a given placement, actual routing can be carried out.

1.6 Previous Work

In the past two decades a vast amount of effort has been directed toward the placement and routing problems. However, until recently, little has been done regarding the estimation of their measures.

Perhaps the earliest reported work on wiring space estimation was that of Sutherland and Oestricher [20], in which simple guidelines were provided for selecting the dimensions of a printed circuit board independent of the circuits to be placed on the board. The theory assumes that components are placed randomly on the board, an assumption appropriate for boards with control logic in which there is little or no regularity and where signals are distributed to widely separated gates.

Assuming a random placement model, their theory shows that the number of wires crossing the midsection of the board is approximately $1/4$ the number of active pins. Using this with the knowledge of wire dimensions and the number of wires blocked by pads, an estimate for the board area is obtained as a function of the number of rows and columns of components. In summary, their theory predicts the minimum board area required for a given number of rows and columns of components. In addition, their theory shows that the area per component increases as the number of components increases. Finally they conclude that the minimum area for any pin configuration is achieved by square boards.

Wiring space estimation for one dimensional layouts of integrated circuits has been considered by Heller et al. [12], in which the probability of

successfully wiring a single row of cells as a function of the number of tracks is determined. Their model assumes knowledge of the average wire length and that the number of wires emerging from a cell is a Poisson distributed random variable with parameter λ . Estimates of λ and the average wire length were derived separately in [5], [8]. The results of the one-dimensional model were applied to a two dimensional array of cells by transforming the latter to two one dimensional problems. This transformation consisted of collapsing some number of cells in a column and row into a single cell resulting in two linear arrays of cells. Values of the number of ports, the average wire length and the number of tracks were modified to reflect the effect of this transformation.

The one-dimensional stochastic model of interconnections described above was extended to two-dimensional layouts of master slice integrated circuits by Gamal [9]. A master slice integrated circuit is viewed as an $N \times N$ lattice of points, with each point representing a logic cell. The space between the rows and columns of lattice points are the horizontal and vertical channels through which wires are routed. The assumptions regarding the wiring process are

1. The number of wires emerging from a lattice point is a Poisson distributed random variable with parameter λ .
2. A wire emerging from a point (i, j) has length $L_{i, j}$ with probability $P_{L_{i, j}}$ and mean R .
3. Wires may follow one of four equally probable rectilinear trajectories.

Based on these assumptions it was shown that the random variables $T_{i, j}^h$, which represent the number of wires in a horizontal channel segment between points (i, j) and $(i+1, j)$, are Poisson distributed. Since the random variables $T_{i, j}^h$ and $T_{k, 1}^v$ are not independent, joint distributions could not be obtained. Instead, bounds on the expected value of the maximum channel width were derived.

The stochastic model of interconnections has been extended to custom ICs by Syed [21]. The earlier assumptions regarding the wire generation and wire length distributions are retained. Additionally, to handle the non-uniform channel topology of custom ICs, a channel graph is constructed to generate estimates of the individual channel dimensions specific to the given topology. The nodes of the channel graph represent the channel intersections and the arcs represent the channels. The width of a channel (arc) is estimated as a function of the number of wires that enter the channel and the number of wires that emerge within the channel and terminate either within the channel or outside the channel. Assuming that a good initial placement is available, channel dimensions are computed and used during the routing phase of chip design. When the estimated channel size is too small, additional tracks are added to complete the routing. It is assumed that the resulting perturbation in the placement due to the addition of tracks is sufficiently small so as to not alter the structure of the channel graph.

The stochastic models of interconnections described so far ignore a number of aspects of the wiring process. In both [9] and [21] a wire emerging from a point (i,j) and terminating at (k,l) contributes equally to all the intermediate channels between (i,j) and (k,l) . A more realistic model would be to assume that a wire from (i,j) to (k,l) would use a given intermediate channel according to the probability of such a wire being incident on that channel. Additionally, the model in [9] treats all channels identically, resulting in bounds on the channel dimensions that are very pessimistic. To support this, let us consider how the bounds on the expected value of the width of the widest channel are computed in [9].

Let T_N denote the width of the widest channel segment. Let $\mathfrak{S}_{i,j}$ denote the joint event $\{T_{i,j}^h < t, T_{i,j}^v < t\}$ and $\mathfrak{S}'_{i,j}$ its complement. Then

$$\begin{aligned}
E\{T_N\} &= \sum_{t=1}^{\infty} P\{T_N \geq t\} \\
P\{T_N < t\} &= P\left\{\max_{(i,j)}(T_{ij}^h, T_{ij}^v) < t\right\} = P\{z_{ij}\} \quad \forall i,j \\
P\{T_N < t\} &= P\{z_{1,1}, \dots, z_{N,N}\} \\
P\{T_N \geq t\} &= P\{z'_{1,1} \cup \dots \cup z'_{N,N}\} \leq \sum P\{z'_{ij}\} = N^2 \cdot P\{z'_{1,1}\} \\
E\{T_N\} &= \sum_{t=1}^{\infty} P\{T_N \geq t\} \leq \sum_{t=1}^{\infty} N^2 (1 - P\{T_{1,1}^h < t, T_{1,1}^v < t\})
\end{aligned}$$

The above inequality was derived using the simple fact that

$$P\left(\bigcup_{i=0}^n A_i\right) \leq \sum_{i=0}^n P(A_i)$$

Clearly, bounds derived using this union of events bound will be quite loose. Finally, no attempt is made to generate estimates of the individual channel capacities.

In [21] procedures for generating individual channel dimension estimates for custom ICs are provided. However, the width and heights of the channels were inaccurately derived, under-estimating the dimensions of the channels. To support this, let us see how the estimate for the width of a channel (i,j) , denoted by $W_{i,j}$, is derived. Let this channel be of length $l_{i,j}$. Let t denote some point along the length of this channel, i.e. $0 \leq t \leq l_{i,j}$ and $W_{i,j}(t)$ denote the number of wires crossing the point t within this channel. Then the width of this channel is given by

$$W_{i,j} = \text{Max}_t (W_{i,j}(t))$$

$W_{i,j}(t)$ is a stochastic process. For each value of t , $W_{i,j}(t)$ represents a random variable and not a deterministic time function of t . To find $E\{W_{i,j}\}$ one must find the distribution of the maximum and then compute the expected value. Instead, the maximum of the expected value of $W_{i,j}(t)$ was computed. In the following lemma we prove that $\text{Max}(E\{W(t)\}) \leq E\{\text{Max}(W(t))\}$ and show that the results in [21] significantly underestimate the channel capacities.

Lemma 1: Let X_1, \dots, X_n be n non-negative random variables having a joint distribution function $F(X_1, \dots, X_n)$. Then

$$E \left\{ \text{MAX}_{1 \leq i \leq n} (x_i) \right\} > \text{MAX}_{1 \leq i \leq n} E\{x_i\}$$

Proof

$$E \left\{ \text{MAX}_{1 \leq i \leq n} (x_i) \right\} = \int \text{MAX}_{1 \leq i \leq n} (x_i) dF(x_1, x_2, \dots, x_n)$$

$$\geq \int x_i dF(x_1, \dots, x_n) \quad \forall i$$

$$E \left\{ \text{MAX}_{1 \leq i \leq n} (x_i) \right\} \geq \text{MAX}_{1 \leq i \leq n} \int x_i dF(x_1, \dots, x_n) = \text{MAX}_{1 \leq i \leq n} E\{x_i\}.$$

Note : In the above lemma equality holds in the degenerate case where all the random variables are identical with probability one.

Some other limitations of earlier models are :

1. Paths with limited vias

In [9] the model of interconnections was modified to consider wires with at most one via. An immediate extension would be to consider wires with at most v vias, where $v \geq 1$.

2. Minimal length paths

All the models discussed so far assumed wires follow minimal length rectilinear paths. However, most routing schemes recognize that quite often it is not possible to achieve 100% routing using minimal length paths and allow nets to deviate a certain amount from the minimal path. In [1] a procedure for generating all paths between two points with a deviation δ is presented. The problem of how the channel dimension estimates vary with δ has not been addressed so far.

1.7 Summary of Report

In this report we develop models for estimating the amount of wiring space needed for master slice ICs. As described earlier several authors, [9], [12], [5], have addressed simpler versions of this problem but were unable to obtain estimates of individual channel capacities. The model described in this report enables us to efficiently compute estimates of individual channel sizes.

The new approaches to wiring space estimation of master slice chips considered in this report are as follows. Wires at the intersection of a

horizontal and vertical channel are classified as belonging to one of six classes. Unlike earlier models, [9], [12], the probability of a wire belonging to one of these classes at each channel intersection is accounted for. Distributions of the number of each type at a channel intersection can be derived. As the dimensions of a channel intersection are functions of the number of wires belonging to each class, expected values of these quantities will be obtained. Based on these, the dimensions of each channel can be computed.

Preliminary results on extending the model to allow wires with a fixed number vias are presented. This problem is interesting for the following reasons. First, each addition of a via decreases the amount of space for routing the wires. Secondly, during fabrication it is possible for the masks with vias and the masks with wires to be misaligned resulting in a faulty circuit. Finally, any possible relationship between v and the congestion in the channels needs to be studied, hence the necessity for the via restriction.

1.8 Outline of report

In the next section our model for interconnections on an MS chip is described. Each wire segment at a channel intersection is classified into one of six classes and both the marginal and joint distributions of these quantities are derived. In addition, each wire uses a channel intersection according to a probability of such a wire being incident at that channel intersection. Using these weighted paths and knowledge of the distributions of the various classes of wire segments, exact expressions for the width and height of a channel are derived. Finally, some initial results on paths with fixed numbers of vias are also presented.

2 Channel Capacity Estimation of MS IC's

In this section we present a refinement over earlier models of interconnections on a master-slice integrated circuit to obtain accurate estimates of individual channel capacities.

A master-slice chip is an $N \times N$ array of equal size logic cells (see figure 1a) which is represented as a two-dimensional lattice of points, where each point corresponds to the intersection of a horizontal and vertical channel (see figure 1b).

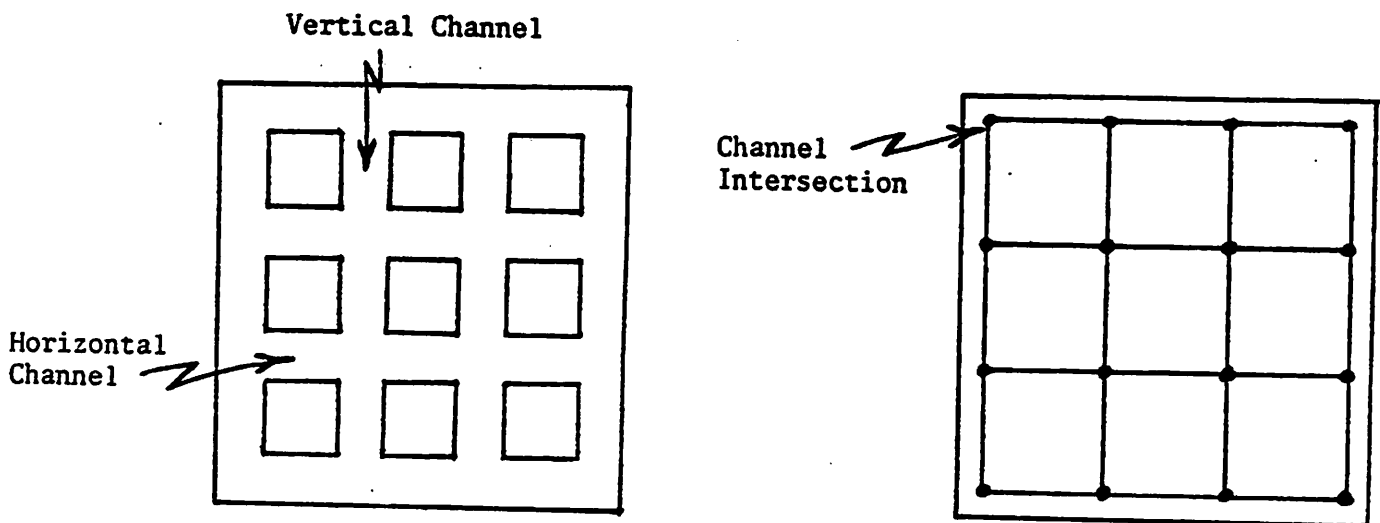


Figure 1: View of a MS chip

2.1 Assumptions

The model assumes :

1. The number of wires $X_{i,j}$ emerging from location (i,j) is a Poisson distributed random variable with parameter λ .
2. Wires emerge and terminate at channel intersections and follow minimal rectilinear paths between source and destination points.
3. All minimal paths between points (i,j) and (k,l) do not contribute equally to an intermediate channel intersection (r,s) , but rather the contribution depends on the relative locations of (i,j) , (k,l) and (r,s) .

2.2 Notation and Definitions

1. A connection between two points (i,j) and (k,l) can belong to one of two classes. We define a forward wire to be one where $i \leq k$ and $j \leq l$. Similarly, a backward wire is one where $i \leq k$ and $j > l$. These two classes are depicted in figure 2.
2. A wire between (i,j) and (k,l) can behave in a number of ways within a channel intersection (r,s) . These are depicted in figure 3 and labelled as class 1, class 2, etc.

3. We define

$X_{i,j}$	= number of wires emerging from location (i,j) .
$X_{i,j}^{k,l}$	= number of wires emerging from location (i,j) and terminating at (k,l) .
$Y_{i,j,t}^{k,l}(r,s)$	= number of wire segments that belong to class t , ($t = 1, 2, \dots, 6$), at (r,s) contributed by wires emerging at (i,j) and terminating at (k,l) .
$N_{i,j}^{k,l}$	= number of minimal length rectilinear paths between (i,j) and (k,l) .
$q_{i,j}^{k,l}$	= probability that a wire emerging from (i,j) terminates at (k,l) .
$P_{i,j,t}^{k,l}$	= probability that a wire from (i,j) to (k,l) falls into class t , ($t = 1, 2, \dots, 6$), at channel intersection (r,s) .
$W(r,s)$	= width or horizontal dimension of channel intersection (r,s) .
$H(r,s)$	= height or vertical dimension of channel intersection (r,s) .
$T_t(r,s)$	= total number of wire segments in channel intersection (r,s) that belong to class t .

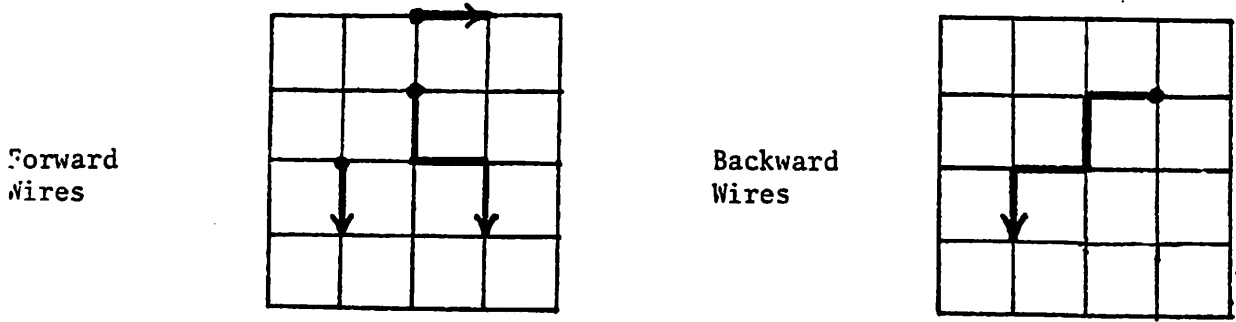


Figure 2: Type of Wires

- 1 - Class 1
- 2 - Class 2
- 3 - Class 3
- 4 - Class 4
- 5 - Class 5
- 6 - Class 6

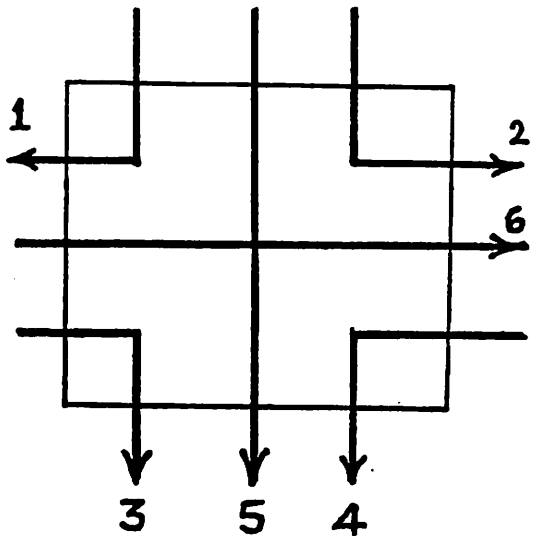


Figure 3: Classes of wire segments in a channel intersection

2.3 Estimation Width and Height

Consider the channel intersection at (r,s) shown in figure 3. Within such a channel intersection a class 1 wire segment may not use the same vertical track as a class 2 wire segment. Similarly, class 3 and class 4 wire segments need distinct vertical track segments. However, class 1 and class 3 (or class 2 and class 4) wire segments can share the same vertical track. Thus, it is easily seen that

$$W(r,s) = \text{Max} \{ T_1(r,s)+T_2(r,s), T_3(r,s)+T_4(r,s) \} + T_5(r,s) \quad (1)$$

$$H(r,s) = \text{Max} \{ T_1(r,s)+T_3(r,s), T_2(r,s)+T_4(r,s) \} + T_6(r,s)$$

Let $Y_{i,j,t}^{k,1}(r,s)$ be the random variable that represents the number of wire segments that belong to class t , ($t = 1, 2, \dots, 6$), at (r,s) contributed by the wires emerging at (i,j) and terminating at $(k,1)$. To obtain expected values of $W(r,s)$ and $H(r,s)$ we need to determine the distribution of the $Y_{i,j,t}^{k,1}$.

2.4 Distribution of $Y_{i,j,t}^{k,1}$

Among the $X_{i,j}$ wires that emerge from (i,j) , $X_{i,j}^{k,1}$ terminate at $(k,1)$. For a given channel intersection (r,s) , some proportions of these $X_{i,j}^{k,1}$ wires fall into the six classes mentioned earlier. These proportions are given by $p_{i,j,t}^{k,1}$ for $t = 1, 2, \dots, 6$. The joint probability that the six random variables $(Y_{i,j,1}^{k,1}, \dots, Y_{i,j,6}^{k,1})$ having values (y_1, \dots, y_6) given $X_{i,j}^{k,1}$, is equivalent to the probability of observing six mutually exclusive events, E_1, \dots, E_6 , with event E_i occurring y_i times in $X_{i,j}^{k,1}$ independent drawings. This probability is given by the multinomial distribution. Thus we have :

$$P \left\{ Y_{i,j,1}^{k,l}(r,s) = y_1, \dots, Y_{i,j,6}^{k,l}(r,s) = y_6 \mid X_{i,j}^{k,l} \right\} = \frac{X_{i,j}^{k,l}}{y_1! y_2! \dots y_6! y_7!} (p_1)^{y_1} (p_2)^{y_2} \dots (p_6)^{y_6} (p_7)^{y_7}$$

$$\text{where } p_{i,j,7}^{k,l}(r,s) = 1 - \sum_{t=1}^6 p_{i,j,t}^{k,l} \quad (2.2)$$

$$\text{and } y_7 = X_{i,j}^{k,l} - \sum_{t=1}^6 y_t$$

The following theorem shows that if k random variables Y_1, \dots, Y_k , conditioned on N , are multinomially distributed with parameters N and p_1, \dots, p_k then the joint unconditional distribution of (Y_1, \dots, Y_k) is a product of the marginals, each of which is Poisson distributed with parameter λp_i .

Theorem 2: Let Y_1, Y_2, \dots, Y_k be k random variables having a multinomial distribution with parameters N and p_1, p_2, \dots, p_k . If $N = \text{Poisson}(\lambda)$ then

$$P \left\{ Y_1, \dots, Y_k \right\} = \prod_{i=1}^k \frac{(\lambda p_i)^{y_i} e^{-\lambda p_i}}{y_i!}$$

Proof

$$\text{Let } Y_{k+1} = N - \sum_{i=1}^k Y_i, \quad P_{k+1} = 1 - \sum_{i=1}^k p_i$$

$$P \left(Y_1, Y_2, \dots, Y_k \right) = \sum_{N=0}^{\infty} P \left(Y_1, Y_2, \dots, Y_k \mid N \right) P(N)$$

$$\begin{aligned}
&= \sum_{N=0}^{\infty} \left(\frac{N!}{y_1! y_2! \dots y_k! y_{k+1}!} (p_1)^{y_1} (p_2)^{y_2} \dots (p_k)^{y_k} (p_{k+1})^{y_{k+1}} \right) \frac{\lambda^N e^{-\lambda}}{N!} \quad (2.3) \\
&= \sum_{N=0}^{\infty} \left(\prod_{i=1}^k \frac{(\lambda p_i)^{y_i}}{y_i!} \right) \left[\frac{(\lambda(1-p_1-p_2-\dots-p_k))^{N-y_1-\dots-y_k} e^{-\lambda}}{(N-y_1-y_2-\dots-y_k)!} \right] \\
&= \left(\prod_{i=1}^k \frac{(\lambda p_i)^{y_i}}{y_i!} e^{(-\lambda p_i)} \right)
\end{aligned}$$

We see that the joint distribution of Y_1, \dots, Y_k , is a product of the marginals. That is, when the number of trials is itself a random variable with a Poisson distribution, the random variables denoting the numbers of each type of event in a given cell become independent. It is this powerful property that enables us to analyze the wiring process.

Lemma 3: Given $X_{i,j}$ is Poisson distributed with parameter λ , then $X_{i,j}^{k,l}$ is Poisson distributed with parameter $\lambda q_{i,j}^{k,l}$, where $q_{i,j}^{k,l}$ is the probability that a wire originating at (i,j) terminates at (k,l) .

Proof

Let a wire originating at (i,j) and terminating at (k,l) correspond to a success and one that does not terminate at (k,l) correspond to a failure. Then the probability that $x_{i,j}^{k,l}$ wires originate at (i,j) and terminate at (k,l) is equal to the probability of observing $x_{i,j}^{k,l}$ successes in $X_{i,j}$ Bernoulli trials. Thus

$$P \left\{ X_{i,j}^{k,l} = x \mid X_{i,j} \right\} = \binom{X_{i,j}}{x} (q_{i,j}^{k,l})^x (1 - q_{i,j}^{k,l})^{X_{i,j} - x}$$

The above is a special case ($N = 2$) of theorem 1. Applying theorem 1 we have

$$P \left\{ X_{i,j}^{k,l} = x \right\} = \frac{e^{-\lambda q_{i,j}^{k,l}} (\lambda q_{i,j}^{k,l})^x}{x!} = \text{Poisson}(\lambda q_{i,j}^{k,l})$$

Since $X_{i,j}^{k,l}$ are Poisson distributed, we can apply theorem 1 again to the joint distribution of $(Y_{i,j,t}^{k,l}, (r,s), t = 1, 2, \dots, 6)$ and obtain the marginal distribution. Thus we have

$$P \left\{ Y_{i,j,t}^{k,l}(r,s) \right\} = \text{Poisson} \left\{ \lambda q_{i,j}^{k,l} = p_{i,j,t}^{k,l}(r,s) \right\}$$

Now the total number of wire segments in cell (r,s) belonging to class t is given by

$$T_t(r,s) = \sum_{(i,j),(k,l)} Y_{i,j,t}^{k,l}(r,s)$$

$T_t(r,s)$ is the sum of independent Poisson random variables. Thus $T_t(r,s)$ is Poisson distributed with parameter

$$\sum_{(i,j),(k,l)} \lambda q_{ij}^{k,l} = p_{ij,t}^{k,l}(r,s)$$

2.5 Determination of $p_{i,j,t}^{k,l}(r,s)$

We defined $p_{i,j,t}^{k,l}(r,s)$ to be the probability that a wire from (i,j) to (k,l) belongs to class t , ($t = 1, 2, \dots, 6$), in cell (r,s) . Consider the lattice shown in figure 4.

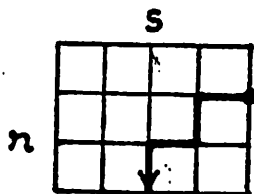


Figure 4: Class 1 wire segment at cell (r,s)

The total number of minimal rectilinear paths from (i,j) to (k,l) is given by

$$N_{ij}^{k,l} = \binom{k-i+l-j}{k-i}$$

Consider $p_{i,j,1}^{k,l}(r,s)$ and a wire with $i \leq r < k$, $1 \leq s < j$. For such a wire to belong to class 1 in cell (r,s) it must go through channel intersections $(r-1,s)$, (r,s) and $(r,s-1)$. The probability of this event is given by

$$p_{i,j,1}^{k,l} = \frac{\binom{r-i-1+j-s}{r-i-1} \binom{k-r+s-l-1}{k-r}}{\binom{k-i+l-j}{k-i}} \quad i \leq r < k, l \leq s < j$$

On the other hand, if $\{(i,j) (k,l)\}$ is a forward wire, i.e. $i \leq k, j \leq l$, then it can never belong to class 1 at any point (r,s) . Thus we have

$$p_{i,j,1}^{k,l}(r,s) = \frac{\binom{r-i-1+j-s}{r-i-1} \binom{k-r+s-l-1}{k-r}}{\binom{k-i+l-j}{k-i}} \quad i \leq r < k, l \leq s < j$$

0 otherwise

Similarly, for a wire from (i,j) to (k,l) to belong to class 2 in (r,s) it must be the case that $i < r \leq k, j \leq s < l$ and it must go through channel intersections $(r-1,s)$, (r,s) and $(r,s+1)$. Thus we have

$$p_{i,j,2}^{k,l}(r,s) = \frac{\binom{r-i-1+s-j}{r-i-1} \binom{k-r+l-s-1}{k-r}}{\binom{k-i+l-j}{k-i}} \quad i < r \leq k, j \leq s < l$$

0 otherwise

By similar observations one can easily obtain the following expressions for the probabilities of the remaining classes of wire segments in (r,s) .

$$p_{i,j,3}^{k,l}(r,s) = \frac{\binom{r-i+s-j-1}{r-i} \binom{k-r-1+l-s}{k-r-1}}{\binom{k-i+l-j}{k-i}} \quad i \leq r < k, j < s \leq l$$

0 otherwise

$$p_{i,j,4}^{k,l}(r,s) = \frac{\binom{r-i+j-s-1}{r-i} \binom{k-r-1+s-l}{k-r-1}}{\binom{k-i+l-j}{k-i}} \quad i \leq r < k, l \leq s < j$$

$$0 \quad \text{otherwise}$$

$$p_{i,j,5}^{k,l}(r,s) = \frac{\binom{r-i-1+|s-j|}{r-i-1} \binom{k-r-1+|l-s|}{k-r-1}}{\binom{k-i+|l-j|}{k-i}} \quad i < r < k$$

$$p_{i,j,6}^{k,l}(r,s) = \frac{\binom{r-i+|s-j|-1}{r-i} \binom{k-r+|l-s|-1}{k-r}}{\binom{k-i+|l-j|}{k-i}} \quad i \leq r \leq k$$

2.6 Determination of $q_{i,j}^{k,1}$

We defined $q_{i,j}^{k,1}$ as the probability that a wire emerging at (i,j) terminates at $(k,1)$. Due to the statistical nature of the wireability analysis carried out here, $q_{i,j}^{k,1}$ is the probability $P_L(d)$ that a wire has length equal to the distance d between the points (i,j) and $(k,1)$. $q_{i,j}^{k,1}$ depends only on the

distance d and not on the specific locations of the points (i,j) and $(k,1)$. Additionally, since placement of components is usually done to realize as few long connections as possible, $P_L(d)$ must be a decreasing function of d . A number of candidates for $P_L(d)$ exist. Some examples are the exponential and geometric distributions, both of which have been used in [9], [21] and [12].

The subject of wire length distributions has received extensive attention recently [21], [9], [12], [5], [8], [6]. In [8], [5] and [6] it was shown, both theoretically and experimentally, that the length distribution is intimately related to an empirical relation known as Rent's Rule. This rule predicts the number of external connections that result from a given number of components. Rent's Rule is formulated as

$$T = A \cdot C^p \quad 0 \leq p \leq 1 \quad (2)$$

where T is the number of external connections, A is the average number of connections per component, C is the number of components and p a positive constant. In [6] it was shown that if Rent's Rule is assumed to hold then the wire length distribution has the form

$$P_L(d) = A(\alpha) \cdot d^{-\alpha} \quad \alpha > 0 \quad (3)$$

The model assumes a hierarchical placement method which consists of successively partitioning a square array of cells horizontally and vertically into groups of 4. The model treats all the components as points on a lattice and assumes all nets are two point nets. Additionally, it assumes that Rent's Rule holds at all levels of the partition hierarchy.

In [8] the same form as (3) for the wire length distribution is derived. A partition function $I(r)$, which is defined as the number of connections beginning in a region whose boundary is a distance r from the origin and terminating outside the region, is derived. $I(r)$ is shown to be a function of the wire length distribution $q(r)$. If $q(r)$ has the form shown in equation (3) above then $I(r)$ is shown to have the form of Rent's Rule.

In this report we study, through simulation, various wire length distributions. Specifically, we examine the results using the geometric distribution as well as distributions of the form shown in equation (3). It should be emphasized that $P_L(d)$ is a design parameter and hence its parameters will be empirically determined for the various chips that will be studied.

2.7 Determination of $E\{W(r,s)\}$ and $E\{H(r,s)\}$

Earlier we showed that $T_t(r,s)$ is a Poisson distributed random variable. From equation (1) we observe that to determine $E\{W(r,s)\}$ we need to determine the expected value of the maximum of two independent Poisson random variables.

Theorem 4: Let X and Y be two independent Poisson random variables with parameters λ and μ respectively. Then

$$E\{\text{Max}(X,Y)\} = \lambda + \mu - \sum_{k=0}^{\infty} I(\lambda, k+1) \cdot I(\mu, k+1)$$

$$\text{where } I(\lambda, k+1) = \frac{1}{k!} \int_0^{\lambda} e^{-t} t^k dt$$

Proof

$$\text{Max}(X,Y) = X + Y - \text{Min}(X,Y)$$

$$\begin{aligned} E\{\text{Min}(X,Y)\} &= \sum_{k=0}^{\infty} P(\text{Min}(X,Y) > k) = \sum_{k=0}^{\infty} P(X > k) P(Y > k) \\ &= \sum_{k=0}^{\infty} \sum_{r=k+1}^{\infty} \frac{e^{-\lambda} \lambda^r}{r!} \sum_{s=k+1}^{\infty} \frac{e^{-\mu} \mu^s}{s!} \end{aligned}$$

$$\text{Let } S(\lambda, k) = \sum_{r=k+1}^{\infty} \frac{e^{-\lambda} \lambda^r}{r!}$$

$$\text{Then } S(\lambda, k) = \frac{1}{k!} \int_0^{\lambda} e^{-t} t^k dt$$

The above integral is the incomplete gamma function symbolized by $\Gamma_{\lambda}(k+1)$.
Thus

$$S(\lambda, k) = \frac{\Gamma_{\lambda}(k+1)}{k!} = I(\lambda, k+1)$$

$$\text{Thus } E(\text{Max}(X, Y)) = \lambda + \mu \cdot \sum_{k=0}^{\infty} I(\lambda, k+1) \cdot I(\mu, k+1)$$

The width and height of the channel intersection at (r, s) is given by

$$E(W(r, s)) = \sum_{t=1}^4 \lambda_t(r, s) \cdot \sum_{k=0}^{\infty} I(\lambda_1(r, s) + \lambda_2(r, s), k+1) I(\lambda_3(r, s) + \lambda_4(r, s), k+1) + \lambda_5(r, s)$$

$$E(H(r, s)) = \sum_{t=1}^4 \lambda_t(r, s) \cdot \sum_{k=0}^{\infty} I(\lambda_1(r, s) + \lambda_3(r, s), k+1) I(\lambda_2(r, s) + \lambda_4(r, s), k+1) + \lambda_6(r, s)$$

Thus we have an expression for the expected value of the width and height of each channel intersection as a function of the numbers of different types of wires at the intersection.

The computation of the above sum does not pose any problems. First, the infinite series converges since the sequence of partial sums is monotonically increasing and bounded. Secondly, only the first few terms of the series contribute significantly. Finally, the incomplete gamma function has been tabulated extensively and excellent approximations are available as canned subroutines on the computer.

2.8 Paths with fixed number of vias

In this section we derive an expression for the number of minimal length rectilinear paths between two points having at most v vias. We will use this result later in estimating channel dimensions subject to this restriction. To start with we solve a simple combinatorial problem which will directly yield a solution to our problem.

Lemma 5: Given n ones and m zeros, ($n > 0$, $m > 0$), and an integer $t > 0$, the number of binary sequences with exactly t transitions is given by

$$a(n,m,t) = 2 \cdot \binom{m-1}{(t-1)/2} \binom{n-1}{(t-1)/2} \quad t \text{ odd}$$

$$\binom{m-1}{(t-2)/2} \binom{n-1}{t/2} + \binom{m-1}{t/2} \binom{n-1}{(t-2)/2} \quad t \text{ even}$$

Proof

We first place the m zeros in a row and then distribute the n ones among them. There are two cases to consider.

Case 1: t is odd

Among the m zeros, there are $m-1$ intermediate places where the ones may appear. Each intermediate place where we place one or more ones results in two transitions. When t is odd, then the sequence must begin or end with a one but not both. Otherwise if the sequence started and ended with ones or zeros then we have an odd number of transitions to realize among the $m-1$ intermediate places. This is impossible since a one in any of the intermediate places results in two transitions.

The number of sequences that begin with a one is the same as those that terminate with a one. Hence we need only count those that begin with a one. Among the $m-1$ intermediate places, we select $(t-1)/2$ of them to place the ones. Let X_i denote the number of ones placed in intermediate place i , for $1 \leq i \leq (t-1)/2$ and let Y_1 denote the number of ones placed at the beginning of the sequence. Then the number of ways to distribute n ones among the $(t+1)/2$ places, $(Y_1, X_1, \dots, X_{(t-1)/2})$, is the number of integral solutions to

$$Y_1 + X_1 + \dots + X_{(t-1)/2} = n$$

subject to $Y_1 \geq 1, X_i \geq 1, 1 \leq i \leq (t-1)/2$

This is given by $\binom{n-1}{(t-1)/2}$.

Thus the number of sequences with t transitions, when t is odd is given by

$$2 \cdot \binom{m-1}{(t-1)/2} \binom{n-1}{(t-1)/2}$$

Case 2: t is even

When t is even, the sequences must begin and end with ones or zeros. We first count those that begin and end with zero. In this case we select $t/2$ intermediate places to distribute the n ones among them, each place receiving at least one one. Thus the number of sequences with an even number of transitions that begin and end with zeros is given by

$$\binom{m-1}{t/2} \binom{n-1}{(t-2)/2}$$

Similarly, the number of sequences that begin and end in ones is given by

$$\binom{m-1}{(t-2)/2} \binom{n-1}{t/2}$$

This completes the proof of the lemma.

QED

We can use the above results to obtain the number of minimal length rectilinear paths between two points (i,j) and (k,l) on a lattice with exactly v vias. Let the horizontal segment on a path be represented by a one and a vertical segment by a zero. Then the number of such paths is equal to the number of binary sequences having $k-i$ zeros and $l-j$ ones with v transitions. This is given by

$$N_{ij}^{k,l}(v) = 2 \cdot \binom{k-i-1}{(v-1)/2} \binom{l-j-1}{(v-1)/2} \quad v \text{ odd}$$

$$\binom{k-i-1}{(v-2)/2} \binom{l-j-1}{v/2} + \binom{k-i-1}{v/2} \binom{l-j-1}{(v-2)/2} \quad v \text{ even}$$

Now the number of paths with at most t vias is simply the sum of $N_{i,j}^{k,l}(v)$, from $v = 1, 2, \dots, t$. Using this we obtain the probabilities $p_{i,j,t}^{k,l}(r,s)$ and $q_{i,j}^{k,l}$ and carry out the analysis as before.

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