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Detectability of CMOS Stuck-Open Faults Using Random and Pseudorandom Test Sequences

SARMA SASTRY, MEMBER, IEEE, AND MELVIN BREUER, FELLOW, IEEE

Abstract—In this paper we present an analysis of CMOS stuck-open faults when tested with a *pseudorandom test sequence*, i.e., a test sequence consisting of some or all of the 2^N test patterns generated by a modified N-bit LFSR. Such a scheme is viewed as *testing without replacement.* When all 2^N test patterns are applied, then such a test sequence is called a *pseudorandom exhaustive test sequence* (PRETS). The alternative scheme is called *random testing*, which corresponds to sampling the population of test vectors *with replacement.* We first show that some stuck-open faults require a single test vector for their detection, while most require an ordered pair of test vectors. A PRETS will detect all stuck-open faults that require a single test vector, but may not necessarily detect all faults that require an ordered pair of test vectors. The results obtained under pseudorandom testing are compared with results obtained under random testing.

We present exact and asymptotic formulas for the probability of detecting a stuck-open fault when testing with and without replacement. We then derive expressions for the *expected test length* under the two testing schemes. Finally, we address the problem of estimating the fault coverage for the two different testing schemes. For this problem we present lower bounds on the expected fault coverage. Numerical evaluations of the analytical results for the above problems are also presented.

I. Introduction

BUILT-IN SELF TEST (BIST) [5]–[7] is a testing methodology where some or all of the test circuitry is included on the chip. One class of BIST schemes generates pseudorandom test vectors on-line, i.e., as they are being applied.

Random testing involves generating a *random* sample of test vectors and applying them to the circuit under test. One common technique to generate such vectors is via a linear feedback shift register (LFSR), which consists of a string of D flip-flops and one or more feedback lines passing through XOR gates [6], [7], [15], [16]. An N-bit LFSR has a period of at most $2^N - 1$ and can easily be modified to generate all 2^N input patterns in order to exhaustively test an N-input combinational circuit, although such a modified circuit is no longer linear. Exhaustive testing often has the advantage of not requiring expensive fault simulation. The modified LFSR technique used for performing exhaustive testing is an attractive BIST scheme as it provides for 100 percent fault coverage of all detectable stuck-at (s-a) faults in combinational circuits which do not produce sequential behavior under the presence of a fault.

The situation where a combinational circuit behaves like a sequential circuit in the presence of a fault causes unique testing problems. CMOS circuits, being a three-state logic technology, exhibit this unique failure mode for certain faults such as *stuck-open* (s-op) faults, which can be caused by missing connections at the gate, drain, or source terminal of a FET [2], [8], [14]. Some of the s-op faults require only a single test vector to be detected, while others require an ordered pair of test vectors. If exhaustive testing is performed, then all s-op faults that require only a single test vector can be detected. However, this is not the case for s-op faults that require an ordered pair of test vectors.

Exhaustive testing techniques are practical for circuits with 20 inputs or less. As with any testing procedure, the objective is to achieve a very high fault coverage. For example, some military projects now require tests which detect at least 99 percent of the s-a faults and 75 percent of the CMOS s-op faults. For large test sets and circuits, it is time consuming to determine fault coverage via simulation. Hence there is a need for developing analytical results to aid in predicting fault coverage for CMOS s-op faults when exhaustive test sequences are used.

II. Outline and Summary of Results

In this paper we focus our attention on the probabilistic analysis of s-op faults when tested with a *pseudorandom test sequence of length m*, i.e., a test sequence consisting of m of the 2^N patterns generated by a modified N-bit LFSR. Such a scheme is referred to as *pseudorandom semiexhaustive testing* or *pseudorandom exhaustive testing*, depending on whether $m < 2^N$ or $m = 2^N$, respectively. A given pseudorandom exhaustive test sequence will be called a PRETS. Pseudorandom testing (either semiexhaustive or exhaustive) is viewed as sampling the population of input vectors without replacement. When sampling the population of input vectors is done *with replacement*, then such a scheme will be referred to simply as *random testing*. The results obtained using pseudorandom testing are compared with results obtained using random testing.

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The authors are with the Department of Electrical Engineering-Systems, University of Southern California, Los Angeles, CA 90089-0781.

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In Section II the nature of stuck-open faults in CMOS circuits are briefly described. Two types of subnetworks, referred to as *series type* (s-type) and *parallel type* (p-type) are identified and it is shown that s-op faults in an s-type network require a single test vector for their detection, while s-op faults in a p-type network require an ordered pair of test vectors for their detection.

In Section IV the detectability of s-op faults in p-type networks under random and pseudorandom testing is analyzed. Exact and asymptotic expressions for the probability of detecting a s-op fault are derived. Additionally, bounds on the probability of detecting a s-op fault are derived. Finally, in support of the theory, numerical results are presented.

In Section V we define a quantity called *tau test length*, (denoted by τ_f), which is a random variable that represents the number of vectors that have to be applied in order to detect a given s-op fault f for the first time. The distribution and expected value of τ_f under random and pseudorandom testing are derived.

In Section VI the problems of estimating the fault coverage for the two testing schemes are addressed. Estimating the s-op fault coverage under pseudorandom testing is an extremely difficult combinatorial problem. Hence conservative approximations for the fault coverage are presented. In particular, lower bounds on the fault coverage under random testing are derived.

For the sake of clarity the proofs of all theorems are omitted from the main body of the text; they are presented in the Appendix.

III. Stuck-Open Faults in CMOS Circuits

Consider the CMOS inverter shown in Fig. 1. Assume that the pFET is permanently s-op (fault f). The truth table for this circuit is shown in Table I, where Z denotes a high impedance state and F^{-1} indicates that the present output is the same as the previous output.

From the truth table we see that it is impossible to set $F = 1$ in the faulty circuit; hence this fault can be modeled as F s-a-0. We assume here that the output F was once set to 0.

Now consider the CMOS gate shown in Fig. 2, which is assumed to be embedded in some larger network C. For the input condition $ABCD = 1\times00$ both the series path A–B and the pull-down network are open. The series path C–D is closed. Hence $F = 1$. If the fault f is present then $F =$ Z or $F = F^{-1}$ because both the pull-up and pull-down networks are open. To test for this fault, the output F must first be set to 0 and then followed by a test vector that sets $F = 1$ by closing only the path C–D and leaving the path A–B open.

Thus to detect f requires an ordered pair of test vectors $(t_0; t_1)$ satisfying the following conditions:

1) t_0 sets $F = 0$
2) (a) t_1 sets $F = 1$
   (b) t_1 closes the path C–D
   (c) t_1 opens the path A–B
   (d) t_1 sets up a sensitized path from F to a primary output in the circuit C.

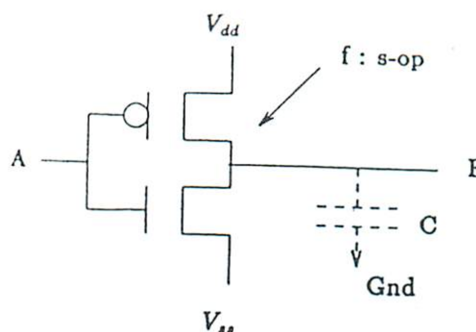

Fig. 1. CMOS inverter.

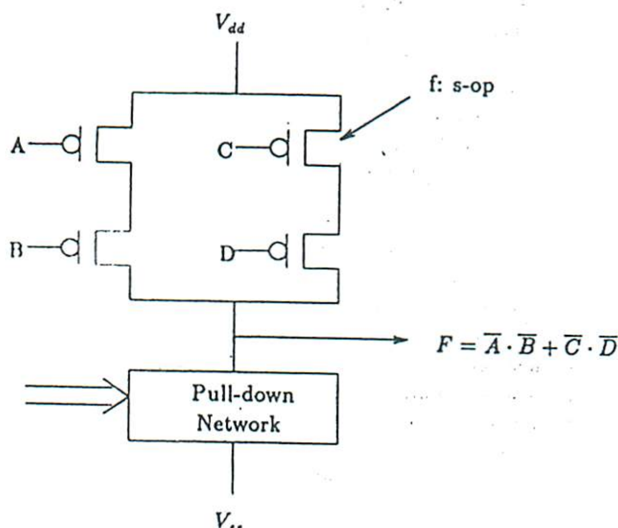

Fig. 2. CMOS gate.

TABLE I
Truth Table for CMOS Inverter

Input A	F Fault Free	F Fault f
0	1	Z or F^{-1}
1	0	0

Condition 2) states that t_1 is a test for F s-a-0 and t_1 sets up the condition such that if the fault exists then the pull-up network is open. Hence t_1 must set up the condition which results in all paths being closed in the pull-up network between V_{dd} and F which pass through the p-FET being tested. The test vectors t_0 and t_1 are referred to as the *initialization* and *sensitization* vectors, respectively. Tests invalidated by hazard conditions are not considered in this paper.

A general CMOS gate consists of the structure shown in Fig. 3. The pull-up network provides a closed path from V_{dd} (logic 1) to the output F for all input vectors $\tilde{x}$, where $F(\tilde{x}) = 1$. Similarly, the pull-down network provides a closed path from the output F to V_{ss} (logic 0) for all input vectors $\tilde{x}$, where $F(\tilde{x}) = 0$.

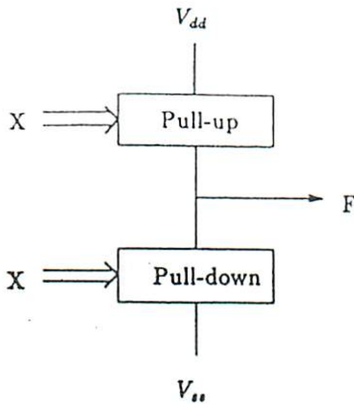

Fig. 3. General structure of a CMOS gate.

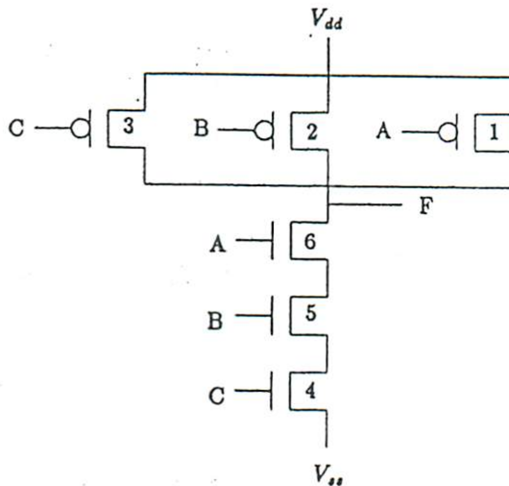

Fig. 4. CMOS NAND gate with three inputs.

Definition 1: A two-terminal pull-up or pull-down network is said to contain a parallel subnetwork, referred to as a p-type network, if there is more than one path between the two terminals going through the subnetwork. A network which is not a p-type network is referred to as an s-type network.

Referring to Fig. 4, the pull-up network is a p-type and the pull-down is an s-type.

From the preceding two examples we see that a s-op fault in an s-type network can be modeled by the s-a model and requires only a single test vector for detection [14]. On the other hand, a s-op fault in a p-type network requires an ordered pair of test vectors for detection. We summarize these observations below.

In an s-type subnetwork within a pull-up network a s-op fault in a p-FET can be modeled by F s-a-0. Similarly, in an s-type subnetwork within a pull-down network a s-op fault in an n-FET can be modeled as F s-a-1. Thus any s-op fault in an s-type CMOS subnetwork can be modeled by a s-a gate fault.

To test for a s-op fault in a p-type pull-up (pull-down) network associated with a gate F within some circuit C, a two-vector sequence t_0, t_1 is required, where t_0 initializes the output of the gate F to 0(1) and t_1 is a test for F s-a-0 (s-a-1) and sensitizes a path from the site of the fault to F.

IV. Probabilistic Analysis of Detection of S-OP Faults

A. Introduction

In this section we analyze the detectability of s-op faults in p-type CMOS combinational networks under *pseudorandom* testing. As stated earlier, pseudorandom testing may be viewed as sampling *without replacement*, i.e., selecting one of 2^N possible test vectors of an N-input circuit at random and applying it to the circuit under test, never repeating the selection.

To see the basic differences between random and pseudorandom testing, consider an N-input combinational network and assume that any one of k test vectors detects a given fault f. Let $n = 2^N$. There are (C_m^{n-k})[1] ways that none of the k vectors will be selected in m trials under pseudorandom testing. Thus the probability of detecting f is given by

$$P_d^{w/o}(k, n, m) = 1 - \frac{\binom{n-k}{m}}{\binom{n}{m}}. \tag{1}$$

Under random testing the probability of not selecting any of the k vectors in m trials is $(1 - k/n)^m$. Thus the probability of detecting f in m trials under random testing is given by

$$P_d^{w}(k, n, m) = 1 - \left(1 - \frac{k}{n}\right)^m. \tag{2}$$

Note that in the latter case it is possible to generate more than n test vectors and not detect f. The probability of this is $(1 - k/n)^n$. For large m these two formulas will be almost identical. Equations (1) and (2) were also derived in [16], where an analysis of random testing for stuck-at faults is presented.

If $m = n$ in (1) (e.g., a PRETS), then $P_d^{w/o}(k, n, n) = 1$. Thus if a PRETS is applied to detect a s-op fault in an s-type network, then the probability of detection is 1. However, this is *not* the case when testing for a s-op fault in a p-type network.

As an example, consider the CMOS circuit shown in Fig. 4 and the fault f_4 defined by n-FET #4 being s-op. It is assumed that F was set to one at some time and has not discharged. Under fault f_4, F can never be zero. Hence f_4 is equivalent to F s-a-1, which is detected by the test vector $(ABC) = (111)$. To detect this fault, suppose a random sample of size m (with replacement) is taken and applied. Then the probability of detecting f_4 is $1 - (1 - 1/8)^m$. If $m = 8$ then this evaluates to 0.344 and the probability of requiring more than eight test vectors to detect f_4 is 0.656. If testing is done using a PRETS, then the probability of detecting f_4 is 1.

Now consider the fault f_1 defined by p-FET #1 being s-op. To detect f_1 requires an ordered pair of test vectors,

[1] Binomial coefficient.

(t_0, t_1), where t_0 sets $F = 0$ and t_1 closes the path with the faulty p-FET and opens all other paths in the pull-up network. There is only one choice for t_0, namely $(ABC) = (111)$, and only one choice for t_1, namely $(ABC) = (011)$. If a PRETS is applied then the probability of detecting f_1 is 0.125. This is arrived at as follows: The pair t_0, t_1 must occur in one of the seven positions $(i, i + 1)$, for $1 \leq i \leq 7$, and there are 6! permutations of the remaining six test vectors. Thus there are 7! PRETS that can detect f_1. Since the total number of PRETS is 8!, the probability of detecting f_1 is $7!/8! = 0.125$. Note that if f_1 has been detected, then f_2 and f_3 are undetectable since there is only one choice for t_0.

Under random testing, testing can proceed indefinitely and the detection of any one of f_1, f_2, or f_3 does not prevent the detection of another. However, if the number of test vectors that are applied is eight, then the probability of detecting f_1 is 0.106, which is smaller than the probability of detection using a PRETS. This is generally the case; that is, the probability of detection using pseudorandom testing will be greater than the probability of detection using random testing for the same number of samples m where $m \leq n$. It can be shown that the expected number of s-op faults detected in the pull-up network of Fig. 4 using a PRETS is 0.375, while using random sampling with $m = n$, it is 0.355. However, as $m \to \infty$ the expected number of faults detected using random sampling is 3.

B. Notation

For the sake of conciseness and clarity the following notation will be used throughout the remainder of this paper:

- N — Number of inputs of a combinational circuit.
- n — Total number of input combinations $= 2^N$.
- f_i — Denotes some s-op fault. When the fault being considered is clearly identified, the subscript will be dropped.
- T_{0i} — Nonempty set of initialization vectors associated with fault f_i.
- T_{1i} — Nonempty set of sensitization vectors associated with fault f_i.
- k_{0i}, k_{1i} — Cardinality of sets T_{0i} and T_{1i} with $2 \leq k_{0i} + k_{1i} \leq n$.
- $P^{w/o}$ — Probability expression under pseudorandom testing (w/o indicates sampling without replacement).
- P^{w} — Probability expression under random testing (w indicates sampling with replacement).
- $\bar{\xi}$ — Complement of some *event* ξ.
- $(x)_j$ — $= x(x-1) \cdots (x-j+1)$.
- $[x]_j$ — $= x(x+1) \cdots (x+j-1) = (-1)^j(-x)_j$.

C. Probability of Detection Using Pseudorandom Testing

In the previous example there was only one candidate for t_0 and t_1. This need not be true in general. The set of vectors satisfying the conditions for t_0 are those that result in $F = 0$ and this set can be quite large. However, in general, the set of vectors that satisfy the conditions for t_1 is relatively much smaller since these vectors must result in $F = 1$ *and* sensitize a path involving the p-FET being tested to the primary output. The following theorems provide general formulas for the probability of detecting a s-op fault in a p-type network under pseudorandom testing. For simplicity we will consider pull-up networks. Similar analysis holds for pull-down networks.

Theorem 1: Let f denote a s-op fault in an N-input CMOS combinational network that requires an ordered pair of vectors (t_0, t_1) to be detected. Let $m^* = \min(k_0, k_1, \lfloor m/2 \rfloor)$. Then the probability of detecting f using m test vectors selected without replacement is given by

$$P_d^{w/o}(k_0, k_1, n, m) = 1 - \sum_{j=0}^{m^*} (-1)^j \binom{m-j}{j} \cdot \frac{(k_0)_j (k_1)_j}{(n)_{2j}}. \quad (3)$$

The parameters k_0 and k_1 are functions of the circuit structure and the fault under consideration. For an arbitrary CMOS gate the space of test vectors is depicted in Fig. 5, where X and Z are the initialization and sensitization sets of a s-op fault, respectively.

For $m < n$ (3) does not have a simple closed form. However, a tight lower bound on $P_d^{w/o}(k_0, k_1, n, m)$ for $m \leq n$ can be obtained. This is stated in the following lemma.

Lemma 1: Let $q = k_0 k_1 / n^2$. Then

$$P_d^{w/o}(k_0, k_1, n, m) \geq 1 - e^{-(m-1)k_0 k_1/n(n-1)} = 1 - e^{-(m-1)(n/n-1)q}. \quad (4)$$

The term q in the lower bound is the product of k_0/n and k_1/n, which represent the probabilities that a randomly selected vector satisfies the conditions for an initialization and a sensitization vector, respectively. Hence q measures the *detectability* of a s-op fault. Since $k_0 + k_1 \leq n$, $q \leq 0.25$. To examine the quality of the bound given in (4), values of $P_d^{w/o}(k_0, k_1, n, m)$ and the lower bound were computed for $n = 64$ and for various values of q and m. Table II shows the exact values of $P_d^{w/o}(k_0, k_1, n, m)$ and the relative error between $P_d^{w/o}(k_0, k_1, n, m)$ and the lower bound given in (4). From the table we see that the lower bound provides an accurate estimate of $P_d^{w/o}(k_0, k_1, n, m)$, especially for faults that are hard to detect (small values of q) or when the number of trials is much smaller than n.

If testing is done exhaustively, i.e., $m = n$ in the statement of Theorem 1, then a simple closed-form expression for $P_d^{w/o}(k_0, k_1, n, m)$ can be derived. This is stated in the following corollary:

Corollary 1: If testing is done using a PRETS, i.e., $m = n$ in the statement of Theorem 1, then

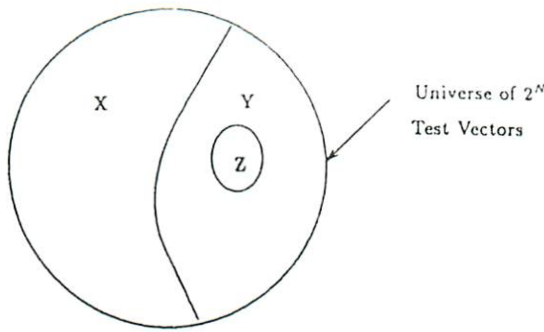

Fig. 5. Space of test vectors.

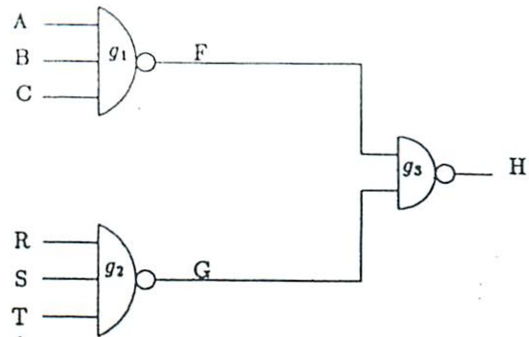

Fig. 6. Two-Level NAND network.

TABLE II
$P_d^{w/o}$ AND RELATIVE ERROR BETWEEN LOWER BOUND WITH $n = 64$

m	4		8		16		32		64	
q	$P_d^{w/o}$	Error	$P_d^{w/o}$	Error	$P_d^{w/o}$	Error	$P_d^{w/o}$	Error	$P_d^{w/o}$	Error
0.002	0.006	0.003	0.014	0.007	0.030	0.015	0.062	0.030	0.125	0.060
0.043	0.129	0.050	0.281	0.062	0.516	0.069	0.794	0.067	0.973	0.038
0.070	0.210	0.080	0.433	0.092	0.720	0.087	0.944	0.056	0.999	0.010
0.098	0.289	0.108	0.567	0.117	0.854	0.094	0.990	0.037	1.000	0.002
0.125	0.365	0.133	0.673	0.125	0.919	0.074	0.996	0.016	1.000	0.000
0.164	0.473	0.168	0.800	0.139	0.974	0.058	1.000	0.005	1.000	0.000
0.203	0.577	0.200	0.894	0.146	0.994	0.040	1.001	0.002	1.000	0.000
0.242	0.678	0.230	0.960	0.144	1.000	0.025	0.992	0.000	1.000	0.000

$$P_d^{w/o}(k_0, k_1, n, n) = 1 - \frac{\binom{n-k_1}{k_0}}{\binom{n}{k_0}} \approx 1 - (1 - k_1/n)^{k_0}. \quad (5)$$

In general, the typical sizes of circuits being tested with PRETS will range from $N = 10$ to $N = 20$. For such large values of n ($n = 2^N$), with $m = n$, (5) provides a simple and excellent approximation to $P_d^{w/o}(k_0, k_1, n, m)$. As an example, consider the two-level NAND circuit shown in Fig. 6. Gate g_1 is the same gate shown in Fig. 4.

Let f denote the fault defined by p-FET #1 of gate g_1 being s-op (see Fig. 4). The set T_0 consists of inputs $\bar{x}$ such that $F(\bar{x}) = 0$. Thus $k_0 = 8$. The set $T_1 = \{\bar{x} | A = 0, B = C = 1, G = 1\}$. Hence $k_1 = 7$. Finally, $n = 2^6 = 64$. From (5) we find the probability of detecting f to be

$$P_d^{w/o}(k_0, k_1, n, n) = 1 - \frac{\binom{57}{8}}{\binom{64}{8}} = 0.6266.$$

Using the approximation to $P_d^{w/o}(k_0, k_1, n, m)$ given in (5), we find

$$P_d^{w/o}(k_0, k_1, n, n) = 1 - (1 - 1/8)^7 = 0.6073.$$

A test for one of the s-op faults in the pull-up network of gate g_3 requires $T_0 = \{\bar{x} | H = 0\}$ and $T_1 = \{\bar{x} | F = 0, G = 1\}$. Thus $k_0 = 49$ and $k_1 = 7$. Using (5) we obtain $P_d^{w/o}(k_0, k_1, n, n) = 0.99998$, while the approximation given by (5) yields 0.99996.

Equation (4) or (5) can be used to determine the value of m necessary for achieving a predefined probability of detection under pseudorandom testing. Note that the parameters k_0, k_1, and n depend on the circuit structure and the fault under consideration, and hence are fixed. Using (4) we solve the inequality

$$P_d^{w/o}(k_0, k_1, n, m) \approx 1 - e^{-(m-1)(n/n-1)q} \geq \alpha \quad (6)$$

which yields

$$m \geq 1 + \left(\frac{n-1}{n}\right)\frac{1}{q} \ln\left(\frac{1}{1-\alpha}\right). \quad (7)$$

The ratio k_0/n represents the fraction of input vectors that result in a 0 at the output. As stated earlier, this fraction is quite large in practice. If an estimate of this is known, then the number of sensitization vectors (k_1) required to obtain a probability of detection of at least α can be obtained from (6). Table III shows such values for $\alpha = 0.99$ when testing is exhaustive, i.e., a PRETS is applied. For example, if it is known that the proportion of initialization vectors is approximately 0.5, then only nine sensitization vectors are needed to detect the fault with a probability of $\alpha = 0.99$, independent of the size of the circuit. The quantity α is often called the *test confidence* and $(1 - \alpha)$ is called the *escape probability*.

Now consider the more general structure of a p-input NAND gate Q embedded in some large circuit shown in Fig. 7. The *cone of logic L* shown in the figure defines the set of i inputs that affect the output of Q. Of the 2^p possible input combinations to Q only one will produce an output of 0. Assume now that this fraction is maintained at the i primary inputs of the cone L. Thus the number of primary input combinations that produce a 0 at the output of Q is $k_0(Q) = 2^{i+j-p} = n2^{-p}$. A typical value of p lies between 2 and 3. In general $p \leq 5$. For $p = 5$ and $n = 2^{20}$ (i.e., a 20-input circuit), $k_0(Q) = 2^{15}$. Hence, one may assume that there are numerous initialization vectors. However, the number of sensitization vectors, $k_1(Q)$, will be far fewer. For the analysis here we have assumed a rather pessimistic situation. An optimistic model would assume that all lines are equally likely to be 0 or 1, and hence $k_0(Q) = 2^{N-1}$.

We can use (7) to obtain a *conservative* bound on the

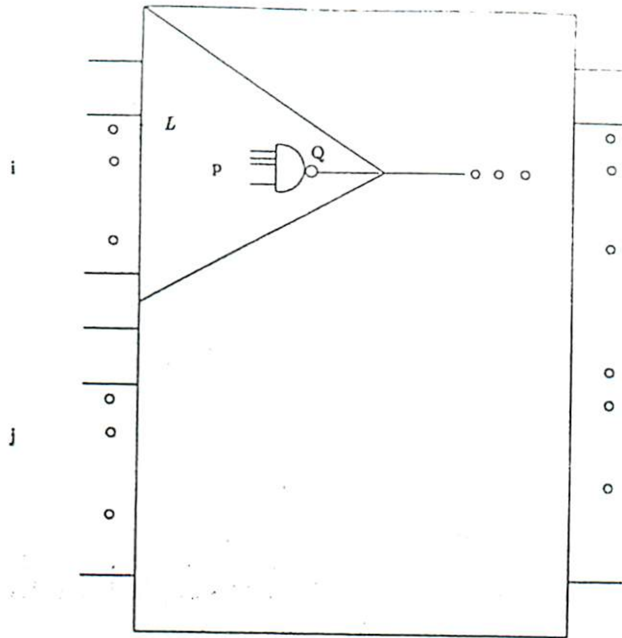

Fig. 7. Gate Q and its cone of logic L.

TABLE III
VALUES OF k_0/n AND k_1 FOR PROBABILITY OF DETECTION ≥ 0.99 USING A PRETS

k_0/n	k_1
.01	≥ 460
.05	≥ 92
.1	≥ 46
.5	≥ 9
.7	≥ 6

number of sensitization vectors needed to achieve a probability of detection $\geq \alpha$ when applying a PRETS ($m = n$). From (7) we find this value to be

$$k_1(Q) \geq 2^p \ln\left(\frac{1}{1-\alpha}\right). \tag{8}$$

Thus using a PRETS to achieve a fault coverage of ≥ 0.95 for a 20-input circuit with $p \leq 5$, the number of sensitization vectors for any fault need not be greater than 94, which is a relatively small fraction of the total number of input combinations.

D. Probability of Detection of S-OP Faults Under Random Testing

In this section we present expressions for the probability of detecting a s-op fault under random testing and provide a comparison with results obtained under pseudorandom testing.

Theorem 2: Let $q = (k_0k_1)/n^2$. Under random testing the probability of detecting f using m test vectors is given by

$$P_d^{w/o}(k_0, k_1, n, m) = \begin{cases} 1 - \dfrac{1}{\sqrt{1-4q}}\left[\left(\dfrac{1+\sqrt{1-4q}}{2}\right)^{m+1} - \left(\dfrac{1-\sqrt{1-4q}}{2}\right)^{m+1}\right], & q < \dfrac{1}{4} \\ 1 - \dfrac{m+1}{2^m}, & q = \dfrac{1}{4}. \end{cases} \tag{9}$$

Note: Equation (9) is equivalent to equation (1) derived in [12], where the problem of random testing with replacement of delay faults is considered, but the derivation here is entirely different.

In (9), for $q < 0.25$, the quantity $(1 + \sqrt{1-4q})/2$ is the dominant term. This observation yields lower and upper bounds on $P_d^w(k_0, k_1, n, m)$. However, without any significant loss in precision, an algebracially much simpler lower bound can be obtained. This is stated in the following lemma.

Lemma 2: For $q \leq 0.25$,

$$P_d^w(k_0, k_1, n, m) \geq 1 - e^{-(m-1)q}. \tag{10}$$

Table IV shows values of $P_d^w(k_0, k_1, n, m)$ computed using (3) and the relative error between these values and the lower bound given in (10), with $n = 64$.

When testing with a PRETS the number of test vectors is n. The number of test vectors under random testing is m, and m can be less than, equal to, or greater than n. For $m \leq n$, $P_d^{w/o}(k_0, k_1, n, m)$ is always greater than $P_d^w(k_0, k_1, n, m)$. Furthermore, when n is large, there appears to be little or no difference between the two testing schemes. The following theorem expresses the fact that if, as $n \to \infty$ the proportions k_0/n and k_1/n remain fixed, then the probability of detection of a s-op fault when testing without replacement approaches the probability of detection when testing with replacement.

Theorem 3: Let $\lim_{n\to\infty} k_0/n = \lambda_0$ and $\lim_{n\to\infty} k_1/n = \lambda_1$. Then

$$\lim_{n\to\infty} P_d^{w/o}(k_0, k_1, n, m) = P_d^w(k_0, k_1, n, m) \tag{11}$$

where $P_d^w(k_0, k_1, n, m)$ is given by (9) with $q = \lambda_0\lambda_1$.

One possible interpretation of Theorem 3 is as follows. Consider a sequence of circuits, $C_1, C_2, \cdots$, having correspondingly larger and larger numbers of inputs. In each of the circuits, C_i, we select a s-op fault f_i and thereby obtain a sequence of faults $f_1, f_2, \cdots$. If the proportions of the initialization and sensitization vectors associated with this sequence of faults remain fixed, then their detection probabilities under pseudorandom testing approach their detection probabilities under random testing.

To compare pseudorandom and random testing, consider again the previous example of the two-level NAND circuit shown in Fig. 6, where $n = 64$. Consider the faults f_1 and f_2 defined by p-FET #1 associated with input A being s-op and one of the p-FET's in the pull-up network

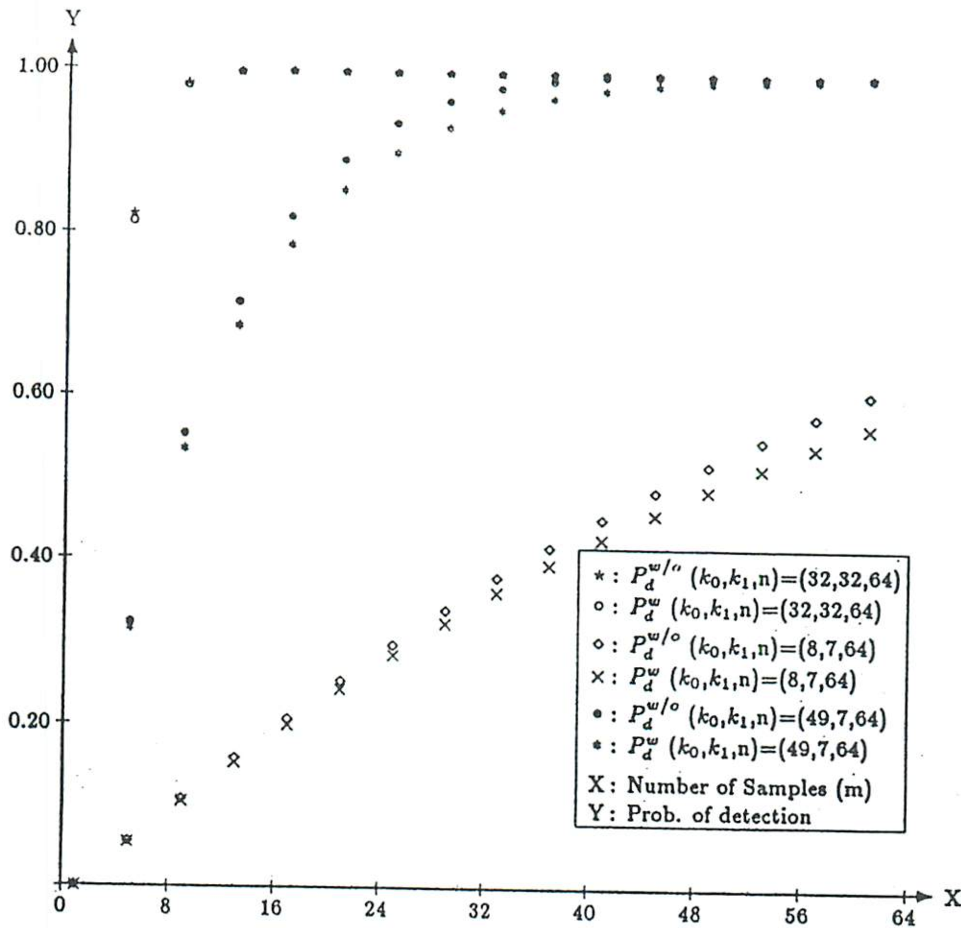

Fig. 8. Probability of detection versus number of samples (m).

TABLE IV
P_d^w AND RELATIVE ERROR BETWEEN LOWER BOUND WITH $n = 64$

m	4		8		16		32		64	
q	P_d^w	Error	P_d^w	Error	P_d^w	Error	P_d^w	Error	P_d^w	Error
0.002	0.006	0.002	0.014	0.003	0.029	0.003	0.059	0.003	0.116	0.003
0.043	0.127	0.048	0.274	0.052	0.498	0.045	0.759	0.031	0.945	0.012
0.070	0.206	0.077	0.421	0.078	0.693	0.059	0.913	0.029	0.993	0.005
0.098	0.283	0.104	0.550	0.099	0.822	0.065	0.972	0.021	0.999	0.001
0.125	0.359	0.130	0.660	0.116	0.904	0.064	0.992	0.013	1.000	0.000
0.164	0.465	0.165	0.788	0.134	0.967	0.054	0.999	0.005	1.000	0.000
0.203	0.568	0.197	0.885	0.143	0.992	0.040	1.000	0.002	1.000	0.000
0.242	0.668	0.227	0.954	0.144	0.999	0.026	1.000	0.000	1.000	0.000

of gate g_3 being s-op, respectively. For fault f_1 we find $k_{01} = 8$ and $k_{11} = 7$, and for fault f_2 we find $k_{02} = 49$ and $k_{12} = 7$. The probability of detecting these two faults as a function of the number of samples (m) under pseudorandom testing ($P_d^{w/o}(k_{01}, k_{11}, n, m)$) and under random testing ($P_d^w(k_{01}, k_{11}, n, m)$) is shown in Fig. 8. Fig. 8 also shows similar plots for $k_0 = k_1 = 32$. These plots indicate that $P_d^{w/o}(k_0, k_1, n, m) \geq P_d^w(k_0, k_1, n, m)$. Furthermore, for a fixed m, the difference between the two testing schemes becomes negligible for large values of k_0 and k_1. This is shown in Fig. 9, where $P_d^{w/o}(k_0, k_1, n, m)$ and $P_d^w(k_0, k_1, n, m)$ are plotted as a function of q for an arbitrary circuit of six inputs and with various values of k_0 and $m = 64$.

V. EXPECTED TEST LENGTH

Two common and useful measures for comparing the quality of different testing schemes are *test length* and *fault coverage*. Test length is defined here to be the number of test vectors that have to be applied to detect a given fault for the first time. The fault coverage of a testing scheme is an indicator of the fraction of all faults that can be detected by the testing scheme. In this section we analyze and evaluate the expected test length under pseudorandom and random testing.

Consider an N-input combinational network and let $n = 2^N$. In the interest of detecting a s-op fault f, suppose a random sample of m test vectors is selected, either with or without replacement, and applied to the circuit. If the fault f is detected, then this detection would have occurred for the first time after the application of the tth vector for some $2 \leq t \leq m$. Consequently, we define a random variable τ_f as follows: If, in the application of the m vectors, fault f is detected for the first time by the $(t - 1)$th and tth vector, for $2 \leq t \leq m$, then τ_f is assigned the value t. On the other hand, if f is not detected, then τ_f is assigned the value m. The random variable τ_f is called the *τ test length* of the fault f. In this section we determine the distribution of τ_f under random and pseudorandom testing.

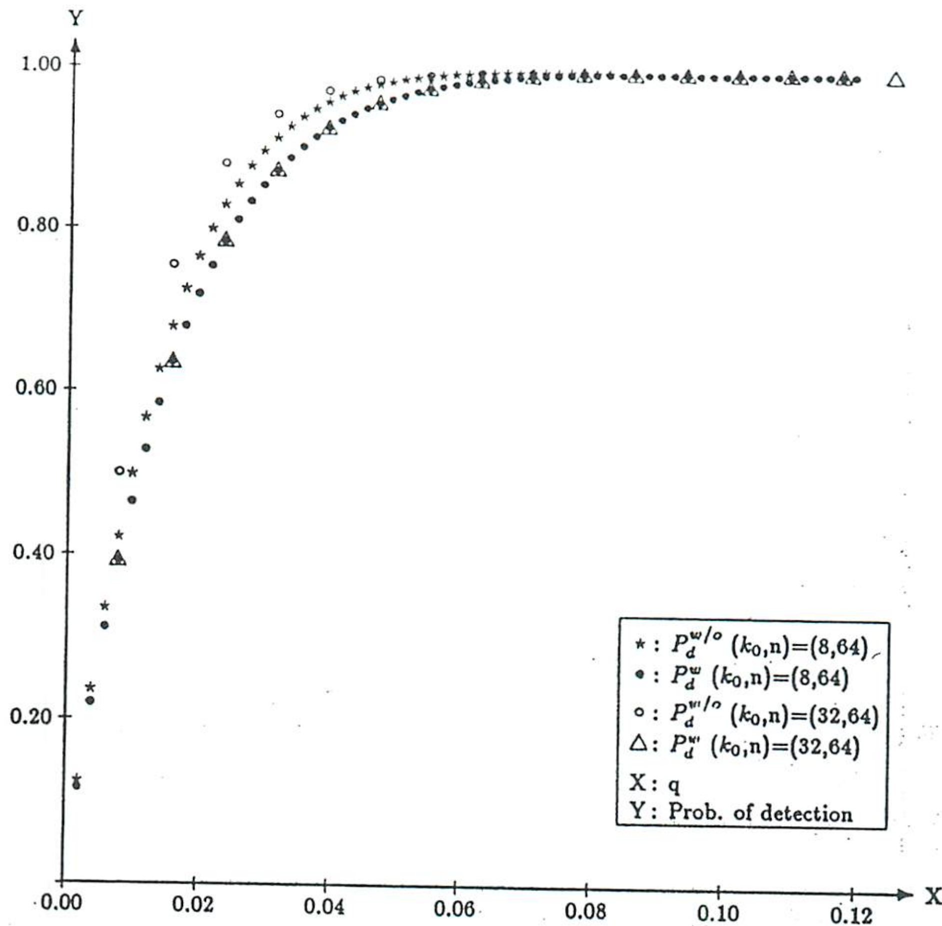

Fig. 9. Probability of detection versus q.

Let η_t denote the event of fault f being detected for the first time by the $(t-1)$th and tth vectors. From the definition of τ_f, we have

$$\{\tau_f = t\} = \begin{cases} \eta_t, & 2 \le t \le m-1 \\ \eta_m \cup \{f \text{ is not detected in } m \text{ trials}\}, & t = m. \end{cases} \quad (12)$$

The events η_t and $\cup_{i=2}^{t} \eta_i$ can be expressed as

$$\eta_t = \bigcup_{i=2}^{t} \eta_i - \bigcup_{i=2}^{t-1} \eta_i \quad (13)$$

$$\bigcup_{i=2}^{t} \eta_i = \{f \text{ is detected in } t \text{ trials}\}. \quad (14)$$

Combining (12), (13), and (14), we obtain

$$P^{w/o}(\tau_f = t|m) = \begin{cases} P_d^{w/o}(k_0, k_1, n, t) - P_d^{w/o}(k_0, k_1, n, t-1), \\ \quad 2 \le t \le m-1 \\ 1 - P_d^{w/o}(k_0, k_1, n, m-1), \quad t = m. \end{cases} \quad (15)$$

In (15) if the superscript w/o is replaced by w, we obtain $P^w(\tau_f = t|m)$. The expression for $P_d^{w/o}(\tau_f = t|m)$ given in (15) and the analogous expression for $P_d^w(\tau_f = t|m)$ can be simplified by using the following recurrences (see the Appendix):

$$P_d^{w/o}(k_0, k_1, n, m) = P_d^{w/o}(k_0, k_1, n, m-1) + \frac{k_0 k_1}{n(n-1)}\left(1 - P_d^{w/o}(k_0-1, k_1-1, n-2, m-2)\right) \quad (16)$$

$$P_d^w(k_0, k_1, n, m) = P_d^w(k_0, k_1, n, m-1) + \frac{k_0 k_1}{n^2}\left(1 - P_d^w(k_0, k_1, n, m-2)\right). \quad (17)$$

Using (15), (16), and (17) we obtain

$$P^{w/o}(\tau_f = t|m) = \begin{cases} \dfrac{k_0 k_1}{n(n-1)}\left(1 - P_d^{w/o}(k_0 - 1, k_1 - 1, n - 2, t - 2)\right), & 2 \le t \le m - 1 \\ 1 - P_d^{w/o}(k_0, k_1, n_1, m - 1), & t = m. \end{cases} \tag{18}$$

$$P^{w}(\tau_f = t|m) = \begin{cases} \dfrac{k_0 k_1}{n^2}\left(1 - P_d^{w}(k_0, k_1, n, t - 2)\right), & 2 \le t \le m - 1 \\ 1 - P_d^{w}(k_0, k_1, n, m - 1), & t = m \end{cases} \tag{19}$$

Recall that m in (18) and (19) represents the number of samples. Thus if a PRETS is applied to the circuit under test, i.e., $m \doteq n$, then the range of τ_f is $2 \le \tau_f \le n$. The expected value of τ_f under pseudorandom testing is given by

$$E^{w/o}(\tau_f) = \sum_{t=2}^{n} t P^{w/o}(\tau_f = t|m = n) \tag{20}$$

which can be computed using (18) and (3).

Now consider the case of random testing. Suppose that the number of samples to be applied to the circuit is *not fixed* and we are interested in determining the expected number of vectors that have to be applied to detect a given s-op fault f for the first time. The range of τ_f is $2 \le \tau_f \le \infty$. From (19) and (9) we have

$$P^{w}(\tau_f = t) = \begin{cases} \dfrac{q}{\sqrt{1-4q}}\left[\left(\dfrac{1+\sqrt{1-4q}}{2}\right)^{t-1} - \left(\dfrac{1-\sqrt{1-4q}}{2}\right)^{t-1}\right], & q < \dfrac{1}{4} \\ \dfrac{t-1}{2^{t-2}}, & q = \dfrac{1}{4}. \end{cases}$$

From (21) one can easily obtain $E^w(\tau_t)$, which is given by

$$E^w(\tau_f) = \frac{1}{q}. \tag{22}$$

In (21), when $q < \frac{1}{4}$, the first term, $(1 + \sqrt{1-4q})/2$, is the dominant term. Using this, we determine the value of t such that $P^w(\tau_f \ge t) \le \epsilon$, for any given ϵ. For $q < \frac{1}{4}$, $P^w(\tau_f \ge t)$ is given by

$$P^w(\tau_f \ge t) = \sum_{i=t}^{\infty} P^w(\tau_f = i) = \frac{1}{\sqrt{1-4q}}\left[\left(\frac{1+\sqrt{1-4q}}{2}\right)^t - \left(\frac{1-\sqrt{1-4q}}{2}\right)^t\right]. \tag{23}$$

Discarding the second term in (23), we find that if

$$t \ge \frac{\ln\left(\epsilon\sqrt{1-4q}\right)}{\ln\left((1+\sqrt{1-4q})/2\right)} \tag{24}$$

then the inequality $P^w(\tau_f \ge t) \le \epsilon$ will be satisfied.

As an example, consider a s-op fault in the pull-up network of gate g_3 shown in Fig. 6, where $n = 64$, $k_0 = 49$, $k_1 = 7$, and $q = 0.0837$. If $\epsilon = 0.01$ then the right-hand side of (24) evaluates to 50. Thus to detect a s-op fault in the pull-up network of gate g_3, the probability that the test length will exceed 50 will be less than 0.01.

To compare $E^{w/o}(\tau_f)$ and $E^w(\tau_f)$, the formulas expressed in (20) and (22) were plotted as a function of q for $n = 64$ with various sizes of the initialization set. This is shown in Fig. 10. From this plot we observe that the expected test length when testing without replacement is always smaller than when testing with replacement. That is, analysis made assuming random testing provides a conservative bound for pseudorandom testing. Referring to Fig. 10, where $n = 64$ and $k_0 = 8$, if $q \ge 0.02$, then the expected number of test vectors needed to detect a given fault is ≤ 30. From the earlier plots, we find that the probability of detecting a fault for $q \ge 0.02$ is ≈ 0.80.

VI. Fault Coverage Under Random Testing

The effectiveness of any test procedure is measured by the percentage of faults that are detected. When applying random test vectors the number of faults detected is a random variable and one is naturally interested in the expected number of faults detected by the application of a random sample of test vectors. Determining the fault coverage under pseudorandom testing poses an extremely difficult combinatorial problem. We are therefore led to the task of obtaining *conservative* approximations. Before we proceed with this task, however, it will be instructive to understand the nature of the difficulty.

Consider the earlier example of the two-level NAND circuit shown in Fig. 6. Assume that we are interested only in faults f_1 and f_7, defined by p-FET's corresponding to input A of gate g_1 and input F of gate g_3 being s-op. The

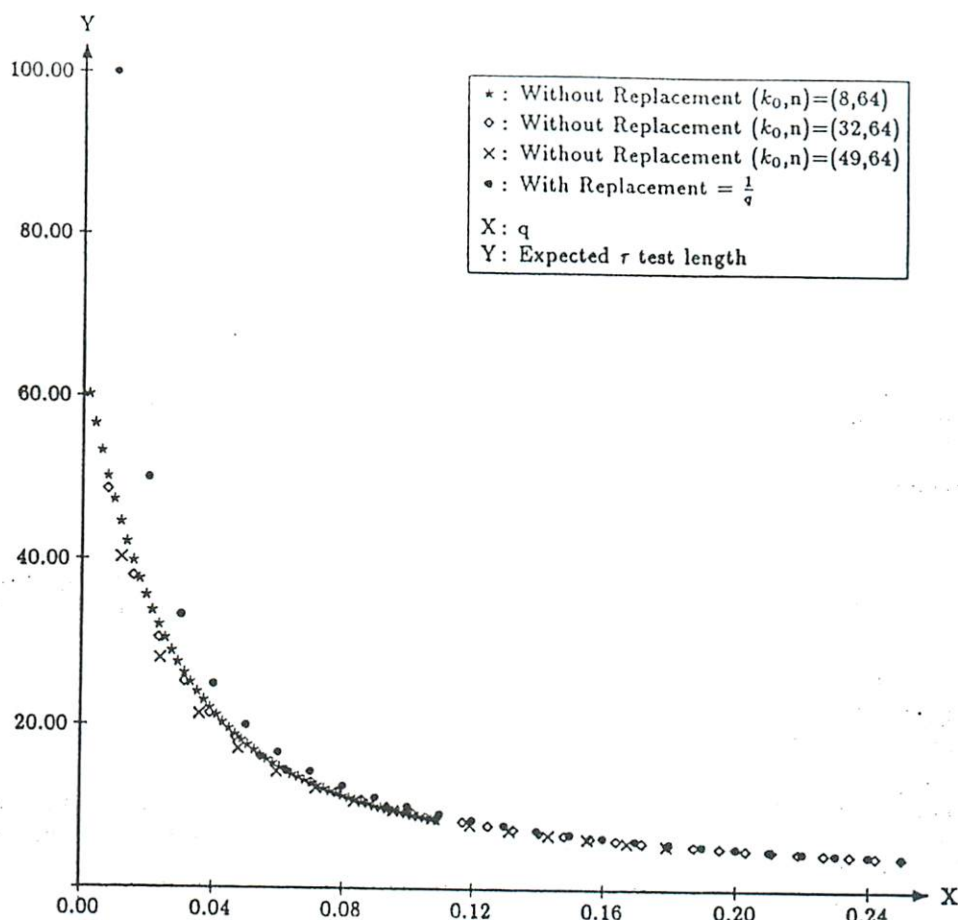

Fig. 10. Expected τ test length versus q.

initialization and sensitization sets for these two faults are given by[2]

$$\begin{aligned}
T_{01} &= \{ABCRST\} = \{111xxx\} && \Rightarrow k_{01} = 8\\
T_{11} &= \{ABCRST\} = \{0110xx,\ 011x0x,\ 011xx0\} && \Rightarrow k_{11} = 7\\
T_{07} &= \{ABCRST\} = \{0xx,\ x0x,\ xx0\} \otimes \{0xx,\ x0x,\ xx0\} && \Rightarrow k_{07} = 49\\
T_{17} &= \{ABCRST\} = \{111xxx,\ xxx111\} && \Rightarrow k_{17} = 15.
\end{aligned}$$

From these initialization and sensitization sets we see that $T_{01} \subset T_{17}$ and $T_{11} \subset T_{07}$. In general, the initialization set of one fault and the sensitization of another fault may have common elements or the initialization and sensitization set of one fault may be subsets of the initialization and sensitization of another fault. Hence the event of one fault being detected may (and often does) depend on the event of another fault being detected. This is the main cause of difficulty in counting the number of ways a randomly selected set of vectors (either with or without replacement) can detect a fixed number (>1) of faults. This task is far more difficult considering that the set of all possible s-op faults that require a pair of test vectors is usually $\gg 2$. In such a case, knowledge of all possible pairwise intersections of the initialization and sensitization sets of each fault is required.

[2] x represents a don't care and $\otimes$ represents the cross product.

We can arrive at a simple lower bound on the expected fault coverage under pseudorandom testing by first considering the expected fault coverage under random testing. To do this, assume that each trial consists of a random selection of a *pair* of test vectors and ignore the possibility that the second vector of some trial i and the first vector of trial $i + 1$ may detect a fault. Let $F = \{f_i\}$, for $i = 1, \cdots, r$, denote the set of all possible s-op faults and ξ_i denote the event that fault f_i is detected on any single trial. Thus on any trial, one of the $r + 1$ possible events $\{\xi_1, \cdots, \xi_r, \xi_{r+1}\}$ may occur, where ξ_{r+1} denotes the event that none of the r faults in F were detected.

Let I_m denote the indicator function, that is,

$$I_m(\xi_i) = \begin{cases} 1 & \text{if } \xi_i \text{ occurs in } m \text{ trials} \\ 0 & \text{otherwise.} \end{cases} \tag{25}$$

In a sequence of m trials conducted with replacement, if ξ_i occurs one or more times, then the fault f_i is detected. Let Y_m denote the number of faults detected in a sequence

of m trials. Hence,

$$Y_m = \sum_{i=1}^{r} I(\xi_i). \tag{26}$$

Let Z_i denote the number of occurences of event ξ_i in m trials with replacement and q_i be the probability of event ξ_i on any trial. Then

$$P\{Z_1 = i_1, \cdots, Z_r = i_r\} = \frac{m!}{i_1! \cdots i_r! i_{r+1}!} q_1^{i_1} \cdots q_r^{i_r} q_{r+1}^{i_{r+1}} \tag{27}$$

where $q_i = k_{0i}k_{1i}/n^2$, $q_{r+1} = 1 - q_1 - \cdots - q_r$ and $i_{r+1} = m - i_1 - \cdots - i_r$.

From (27) it is easy to see that the marginal of Z_i is given by

$$P\{Z_i = i_j\} = \binom{m}{i_j} q_j^{i_j}(1 - q_j)^{m-i_j}. \tag{28}$$

The expected number of faults detected is given by

$$E(Y_m) = \sum_{i=1}^{r} E(I(\xi_i)) = \sum_{i=1}^{r} P\{Z_i \geq 1\}$$
$$= \sum_{i=1}^{r} [1 - P\{Z_i = 0\}] = \sum_{i=1}^{r} [1 - (1 - q_i)^m]$$
$$= r - \sum_{i=1}^{r} (1 - q_i)^m. \tag{29}$$

This leads directly to the following theorem.

Theorem 4: The expected number of faults, ENF, detected in a sequence of m trials under random testing satisfies

$$ENF \geq r - \sum_{i=1}^{r} (1 - q_i)^m. \tag{30}$$

Consider again the two-level NAND network shown in Fig. 6. The total number of s-op faults in the pull-up network is eight. For each such fault the values of q_i were computed and the bound, given by (30), on the expected number of faults detected was found to be 4.72. Thus, the expected fault coverage is ≥59 percent. As expected, this is a very conservative bound.

VII. Summary and Closing Remarks

In this paper we have analyzed the detectability of stuck-open faults in CMOS combinational networks when tested with random and pseudorandom test sequences. Under these two testing schemes we have addressed three basic problems. First, we derived formulas for the probability of detection of s-op faults. Second, we presented formulas for the expected test length under these two testing schemes. Finally, we addressed the problem of determining the fault coverage. In the latter case we derived simple conservative approximations.

All the formulas presented in this paper are functions of the sizes of the initialization and sensitization sets. For a given s-op fault f_i in a p-type pull-up network, the initialization set, T_{0i}, is the set of input vectors that result in a 0 at the output of the faulty gate. The sensitization set, T_{1i}, is the set of input vectors that result in a 1 at the output of the faulty gate and sensitize a path from the site of the fault to a primary output. The sizes of these sets can be estimated by using one of several techniques, such as the statistical fault coverage estimator known as STAFAN [4] or by computing approximations to the signal probabilities using the *cutting algorithm* [11].

By applying all possible pairs of vectors, of which there are n^2, one could theoretically detect all detectable s-op faults. An efficient hardware implementation of a circuit for generating all pairs of vectors (t_0, t_1), where t_0 and t_1 differ in exactly one bit position, has been reported in [1].

Finally, the effect of hazards can invalidate some tests for s-op faults [8]. This phenomenon implies that the effective value of q is actually less than k_0k_1/n^2 and therefore decreases the probability of detection.

Appendix

Proof of Theorem 1: Let $(\mu_1, \mu_2, \cdots, \mu_m)$ be a random selection of m test vectors, without replacement, from the n possible test vectors. Let ξ_i denote the event that $\mu_i \in T_0$ and $\mu_{i+1} \in T_1$ for $1 \leq i \leq m - 1$. We wish to find the probability that there exists at least one index i such that $\mu_i \in T_0$ and $\mu_{i+1} \in T_1$. Thus the probability of detection is given by

$$P_d^{w/o}(k_0, k_1, n, m) = Pr\left\{\bigcup_{i=1}^{m-1} \xi_i\right\}. \tag{A1}$$

Consider the joint event $\{\xi_i \cap \xi_{i+1}\}$, which is, by definition, the event $\{\mu_i \in T_0 \cap \mu_{i+1} \in T_1 \cap \mu_{i+1} \in T_0 \cap \mu_{i+2} \in T_0\}$. Since $T_0 \cap T_1 = \phi$, $\{\xi_i \cap \xi_{i+1}\} = \phi$. Thus for any set of k indices $i_1, i_2, \cdots, i_k$, $P(\xi_{i_1}, \xi_{i_2}, \cdots, \xi_{i_k})$ is zero if any two of the indices are consecutive.

Let $C_{r,m}$ denote the set of r integers chosen from any m consecutive integers such that no two integers in the selection are consecutive. It is easy to show that

$$|C_{r,m}| = \binom{m - r + 1}{r}. \tag{A2}$$

By the principle of inclusion and exclusion we have

$$\left|\bigcup_{i=1}^{m-1} \xi_i\right| = \sum_{j=1}^{\lfloor m/2 \rfloor} \sum_{i_1, \cdots, i_j \in C_{j,m-1}} (-1)^{j-1} \left|\bigcap_{k=1}^{j} \xi_{i_k}\right|. \tag{A3}$$

For a given set of indices $i_1, i_2, \cdots, i_j \in C_{j,m-1}$, $|\cap_{k=1}^{j} \xi_{i_k}|$ can be determined as follows. In positions $i_1, i_2, \cdots, i_j$ we have to place the j elements of T_0. Since T_0 has k_0 elements, this can be done in $(k_0)_j$ ways. In positions $i_1 + 1, i_2 + 1, \cdots, i_j + 1$, we have to place j elements of T_1. This can be done in $(k_1)_j$ ways. Finally, $m - 2j$ elements have to selected from the remaining $n - 2j$ elements. This can be done in $(n - 2j)_{m-2j}$ ways.

Thus we obtain

$$\left|\bigcap_{k=1}^{j} \xi_{i_k}\right| = (k_0)_j (k_1)_j (n-2j)_{m-2j}$$

$$= [n-m+1]_m \frac{(k_0)_j (k_1)_j}{(n)_{2j}}. \qquad \text{(A4)}$$

Substituting the right-hand side of (A4) in (A3) and using the identity given by (A2), we obtain

$$\left|\bigcup_{i=1}^{m-1} \xi_i\right| = [n-m+1]_m \sum_{j=1}^{m^*} (-1)^{j-1} \cdot \binom{m-j}{j} \frac{(k_0)_j (k_1)_j}{(n)_{2j}} \qquad \text{(A5)}$$

where $m^* = \min(k_0, k_1, \lfloor m/2 \rfloor)$. The total number of outcomes is $[n-m+1]_m$. Therefore

$$Pr\left\{\bigcup_{i=1}^{m-1} \xi_i\right\} = \sum_{j=1}^{m^*} (-1)^{j-1} \binom{m-j}{j} \frac{(k_0)_j (k_1)_j}{(n)_{2j}}$$

$$= 1 - \sum_{j=0}^{m^*} (-1)^{j} \binom{m-j}{j} \frac{(k_0)_j (k_1)_j}{(n)_{2j}}. \qquad \text{(A6)}$$

Equation (A6) is the required result. □

Proof of Lemma 1: Let $H(k_0, k_1, n, m) = 1 - P_d^{w/o}(k_0, k_1, n, m)$. Then using the following identity:

$$\binom{n}{k} = \binom{n-1}{k} + \binom{n-1}{k-1} \qquad \text{(A7)}$$

we get

$$H(k_0, k_1, n, m) = H(k_0, k_1, n, m-1) - \frac{k_0 k_1}{n(n-1)} \cdot H(k_0 - 1, k_1 - 1, n-2, m-2)$$

$$H(k_0, k_1, n, 0) = H(k_0, k_1, n, 1) = 1. \qquad \text{(A8)}$$

Keeping k_0, k_1, and n *fixed*, let $h_m = \ln(H(k_0, k_1, n, m))$. Then after taking logarithms, (A8) can be written as

$$h_m = h_{m-1} + y_{m-2} \qquad \text{(A9)}$$

where

$$y_{m-2} = \ln\left(1 - \frac{k_0 k_1}{n(n-1)} \cdot \frac{H(k_0-1, k_1-1, n-2, m-2)}{H(k_0, k_1, n, m-1)}\right). \qquad \text{(A10)}$$

Equation (A9) is a linear recurrence relation in m and yields

$$h_m = \sum_{i=0}^{m-2} y_i$$

$$= \sum_{i=0}^{m-2} \ln\left(1 - \frac{k_0 k_1}{n(n-1)} \cdot \frac{H(k_0-1, k_1-1, n-2, i)}{H(k_0, k_1, n, i+1)}\right)$$

$$= \ln\left\{\prod_{i=0}^{m-2}\left(1 - \frac{k_0 k_1}{n(n-1)} \cdot \frac{H(k_0-1, k_1-1, n-2, i)}{H(k_0, k_1, n, i+1)}\right)\right\}. \qquad \text{(A11)}$$

Using the fact that $\ln(1-x) \le -x$ for $x \le 1$, we obtain

$$h_m \le -(m-1)\frac{k_0 k_1}{n(n-1)}. \qquad \text{(A12)}$$

Combining (A12) with the definition of $H(k_0, k_1, n, m)$ we get the final result. □

Proof of Corollary 1: Replacing m by n in (3), in the statement of Theorem 1, we obtain

$$P_d^{w/o}(k_0, k_1, n, n) = 1 - \sum_{j=0}^{n^*} \binom{n-j}{j} \frac{(k_0)_j (k_1)_j}{(n)_{2j}}. \qquad \text{(A13)}$$

We now state some well-known identities [9] that are used to obtain the final result:

1) $(k_0)_j = (-1)^j [-k_0]_j$

2) $$\binom{n-j}{j} = \frac{(-1)^j [-n]_{2j}}{[-n]_j [1]_j} = \frac{(-1)^j 2^{2j} [-n/2]_j [(-n+1)/2]_j}{[-n]_j [1]_j}$$

3) $(n)_{2j} = [-n]_{2j} = 2^{2j}[-n/2]_j [(-n+1)/2]_j$.

Thus we obtain

$$P_d^{w/o}(k_0, k_1, n, n) = 1 - \sum_{j=0}^{n^*} \frac{[-k_0]_j [-k_1]_j}{[-n]_j [1]_j}. \qquad \text{(A14)}$$

The summation in (A14) is the generalized hypergeometric series [9] of the form ${}_2F_1$. Using the Chu–Vandermonde identity [9] and rewriting the terms as binomial coefficients yields the first part of the result. The approximation given in (5) is easily obtained as follows:

$$\frac{\binom{n-k_1}{k_0}}{\binom{n}{k_0}} = \frac{(n-k_1)(n-k_1-1)\cdots(n-k_1-k_0+1)}{n(n-1)\cdots(n-k_0+1)} = \left(1-\frac{k_1}{n}\right)\left(1-\frac{k_1}{n-1}\right)\cdots \left(1-\frac{k_1}{n-k_0+1}\right). \tag{A15}$$

Replacing each term in the right-hand side of (A15) by the largest term, $(1 - k_1/n)$, yields the final result. □

Proof of Theorem 2: The probability of detection using m test vectors is given by (A1) in the proof of Theorem 1. When sampling with replacement,

$$\left|\bigcap_{k=1}^{j} \xi_{i_k}\right| = k_0^j k_1^j n^{m-2j}. \tag{A16}$$

Substituting the right-hand side of (A16) into (A3) we obtain

$$\left|\bigcup_{i=1}^{m-1} \xi_i\right| = n^m \sum_{j=1}^{\lfloor m/2 \rfloor} (-1)^{j-1}\binom{m-j}{j}\frac{k_0^j k_1^j}{n^{2j}}. \tag{A17}$$

Since the total number of outcomes is n^m, we have

$$P_d^w(k_0, k_1, n, m) = \sum_{j=1}^{\lfloor m/2 \rfloor} (-1)^{j-1}\binom{m-j}{j} q^j = 1 - \sum_{j=0}^{\lfloor m/2 \rfloor} (-1)^{j}\binom{m-j}{j} q^j \tag{A18}$$

where $q = (k_0 k_1/n^2)$. The generating function for the sum on the right-hand side of (A18) is given by

$$F(x) = \frac{1}{1 - x + qx^2}. \tag{A19}$$

By expanding $F(x)$ in a power series and identifying the coefficient of x^m the result is obtained. □

Proof of Lemma 2: The proof of this inequality is identical to the proof of Lemma 1. Let $G(k_0, k_1, n, m) = 1 - P_d^w(k_0, k_1, n; m)$. Then using the identity given in (A7) and (A8), we obtain

$$G(k_0, k_1, n, m) = G(k_0, k_1, n, m-1) - \frac{k_0 k_1}{n^2} \cdot G(k_0, k_1, n, m-2) \tag{A20}$$

$$G(k_0, k_1, n, 0) = G(k_0, k_1, n, 1) = 1. \tag{A21}$$

Keeping k_0, k_1, and n *fixed*, let $g_m = \ln(G(k_0, k_1, n, m))$. Then following the same steps as in the proof of Lemma 1, we obtain

$$g_m = \ln\left\{\prod_{i=0}^{m-2}\left(1 - q\frac{G(k_0, k_1, n, i)}{G(k_0, k_1, n, i+1)}\right)\right\} \tag{A22}$$

where $q = k_0 k_1/n^2$. Again, using the fact that $\ln(1 - x) \leq -x$, we obtain

$$g_m \leq -(m-1)q \tag{A23}$$

which results in

$$G(k_0, k_1, n, m) \leq e^{-(m-1)q}. \tag{A24}$$

Combining (A24) with the definition of G, we obtain the final inequality. □

Proof of Theorem 3: $P_d^{w/o}(k_0, k_1, n, m)$ is given by (A17). Let $\lambda_0 = k_0/n$ and $\lambda_1 = k_1/n$. Then

$$(k_0)_j = n^j \prod_{i=0}^{j} (\lambda_0 - i/n)$$

$$(k_1)_j = n^j \prod_{i=0}^{j} (\lambda_1 - i/n)$$

$$(n)_{2j} = n^{2j} \prod_{i=0}^{j} (1 - i/n)(1 - (j+i)/n).$$

Substituting the above identities into (A17) we obtain

$$P_d^{w/o}(k_0, k_1, n, m) = 1 - \sum_{j=0}^{\lfloor m/2 \rfloor} (-1)^j \prod_{i=0}^{j-1}\left(\frac{\lambda_0 - i/n}{1 - i/n}\right) \cdot \left(\frac{\lambda_1 - i/n}{1 - (j+i)/n}\right)\binom{m-j}{j}. \tag{A25}$$

Let $q = \lambda_0 \lambda_1$. Then

$$\lim_{n\to\infty} P_d^{w/o}(k_0, k_1, n, m) = 1 - \sum_{j=0}^{\lfloor m/2 \rfloor} (-1)^j q^j \binom{m-j}{j}. \tag{A26}$$

The result now follows from Theorem 2. □

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Sarma Sastry (M'85) received the B.M. (honors) degree from the University of Waterl Ont., Canada, in 1976, and the M.S. and Pl degrees in electrical engineering from the U versity of Southern California, Los Angeles, 1980 and 1984, respectively.

At present he is an Assistant Professor Electrical Engineering at U.S.C. His current search interests are in area of design automat of digital systems. These include problems physical chip design, digital system testi hardware verification and the design and analysis of parallel architectu for design automation tasks.

Melvin A. Breuer (S'58–M'65–SM'73–F'85), for a photograph and a b ography, please see p. 798 of this TRANSACTIONS.