**Detecting Multiple Bridging Faults
in CMOS Combinational Circuits***

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Abstract

Monitoring the current supply in CMOS circuits has been shown to be an effective way to detect bridging faults (BFs). In this paper some new results dealing with detecting both single and multiple BFs in combinational CMOS circuits using this current supply monitoring (CSM) method are described. A combinational circuit is partitioned into transistor groups such that in the fault-free circuit, charge sharing effects can occur only among nodes in the same group. A single BF is defined as

redundant if it cannot affect the logic function of a circuit. Three classes of single BFs are then considered. They are BFs inside a group, non-feedback BFs between two groups, and feedback BFs between two groups. It is shown that in all cases, if a single BF cannot be detected using CSM, then it is a redundant fault. It is then shown that if a test vector detects a single BF using CSM, it also detects (using CSM) every multiple BF which contains that single BF. This result implies that a test set which detects all irredundant single BFs also detects all irredundant multiple BFs, where an irredundant multiple BF is defined as a set of BFs containing at least one irredundant single BF. Some SPICE simulation results are also given.

1 Introduction

Detecting bridging faults (BFs) in CMOS circuits by monitoring the current supply has recently attracted much attention[1,2,3]. Three primary reasons for this are: 1) the inadequacy of classic models such as *wired-OR* and *wired-AND* in modelling CMOS bridging faults, 2) the simplicity of test generation using the current supply monitoring method(CSM), and 3) the success in designing *built-in current sensors*(BICS). These three factors are explained below.

The *wired-OR(AND)* model assumes that when two nodes with complemented values are shorted, the resulting voltage on both nodes is logic high(low). This is generally true for TTL and ECL logic. However in a CMOS circuit a bridging fault may force both shorted nodes to take on an intermediate voltage value between VDD and GND which usually cannot be interpreted as a logic high or logic low. As a result, the test based on a *wired-OR(AND)* model may fail to detect a bridging fault. CSM circumvents this dilemma in the following way. During steady state a fault-free circuit should never have a conducting path between VDD and GND and thus only a very small *leakage current* flows. When two nodes, one connected through conducting transistors to VDD and the other to GND, are shorted together, the supply current becomes extremely large. By monitoring this steady state current it is quite likely that this bridging fault will be detected.

It is easy to see that the only requirement for CSM is to set the two shorted nodes to complemented values and measure the supply current. There is no need for fault propagation during test generation. Thus the test generation process is much simpler than that using a wired-OR(AND) model.

The success of CSM depends on the effectiveness of devices for measuring steady-state current. Several researchers have proposed and/or implemented such circuit devices[4,5,6,7]. Built-in current sensors are discussed in [6,7]. Here a circuit is partitioned into modules and a separate BICS for each module is used. This not only facilitates on-line self-testing

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but also makes CSM applicable to complex circuits.

The above discussion suggests that CSM is a promising method for detecting bridging faults in CMOS circuits. Although some detailed examination of BFs in combinational circuits has been done[8,9], a formal proof to show that a *hard short* (a bridging fault with zero resistance) can be detected by CSM has still not appeared. Furthermore, detecting multiple BFs using CSM has not been considered. In this paper three types of single BFs in combinational CMOS circuits are first analyzed. For each type a formal proof is given for the fact that all single irredundant BFs (defined in Section 2) can be detected by CSM. It is then shown that if a test vector detects a single BF, it also detects every multiple BF which contains that single BF. Finally it is concluded that a test set which detects all single irredundant BFs using CSM also detects every multiple BF which contains at least one irredundant single BF. During the analysis SPICE simulation results for both single and multiple BFs are given.

2   CMOS Circuit Modeling and Assumptions

A CMOS circuit is modeled as consisting of a number of n-type/p-type transistors and a number of nodes connecting these transistors. A single BF is allowed to occur between any two nodes. When a BF occurs, it is assumed that the resistance between the two shorted nodes is zero. A single BF is redundant if it has no effect on the logic function of the circuit. To systematically analyze all BFs, a commonly-used partition method for MOSFET circuits is adopted[10,11]. This method partitions a circuit into a number of *transistor groups(TGs)* by breaking the gate terminals of all transistors. Each connected subcircuit after partitioning forms a *TG*. Figure 1(a) shows a partition with each *TGs* indicated by a dotted block. Figure 1(b) is the gate-level representation of this circuit. After partitioning each interconnection among *TGs* is unidirectional and can be considered as an input or output of the corresponding *TGs*. A transistor group *TA* is said to have

direct control on another transistor group *TB* if one of the outputs of *TA* is one of the inputs of *TB*. If there exists a sequence of transistor groups $T_1, T_2, ..., T_n$, $n \geq 2$ such that $TA = T_1$, $TB = T_n$, and T_{i-1} has direct control on T_i for $i = 2, ..., n$, then it is said that *TA* can *control TB*. Two *TGs* are said to be *related* if one of them can control the other. If neither of them can control the other, they are *unrelated*. If both can control each other, then a control loop exists. Most combinational circuits have no control loops.

The following assumptions on a fault-free circuit are made.

A1. The gate node and the drain (or source) node of a transistor cannot be in the same *TG*.

A2. During steady state, there must be no conducting path from *VDD* to *GND*.

A3. During steady state, each output of a transistor group must be connected to *VDD* or *GND* through a path of conducting transistors.

A4. There are no control loops among *TGs*.

A5. The substrate of an *n*-type(*p*-type) transistor is connected to *GND(VDD)*.

A6. Each primary input is controlled by a strong power source whose current flow is also monitored.

A1 is made to exclude the possibility of "self-control" inside a transistor group. A2 is a common attribute of CMOS circuits. A3 ensures that a circuit's normal operation does not rely on any "charge retention" effects. A4 assumes no feedback exists in a combinational circuit. A5 ensures that a BF will not cause *anomalous reverse conduction* [9] which may occur at the drain-substrate junction when the substrate is connected to the source. A6 makes sure that if a primary input is involved in a BF, it cannot change state without consuming a large steady state current, and this abnormal current can be detected.

3   Single Bridging Faults

In this section three categories of single BFs between two nodes in a combinational circuit are analyzed. For each case, the classification of the BF is first given, followed by a lemma and a formal proof that shows each irredundant BF is detectable using CSM. These three lemmas form the basis of Theorem 1. For convenience it is assumed that the BF to be detected occurs between two nodes x and y. To detect such a BF using CSM, x and y must be set to complemented values. Without loss of generality the following discussion assumes that x and y are set to 1 and 0, respectively.

Case 1 *x and y are in the same TG. (Figure 2)*

Lemma 1 *An irredundant single bridging fault satisfying the condition of Case 1 can be detected by using CSM.*

Proof: It suffices to prove that if an input vector T can be found which simultaneously sets up a conducting path P_1 from *VDD* to x and another conducting path P_2 from *GND* to y, then the fault can be detected by using CSM, and if such an input vector does not exist, then the fault is redundant. First assume T can be found. When applying T to the fault-free circuit, no conducting path from *VDD* to *GND* exists and x, y have complemented logic values during steady state . For the faulty circuit in which x and y are shorted, a conducting path forms from *VDD* to *GND* and a voltage redistribution (such that x and y are at the same voltage level) along this path occurs. If such a voltage redistribution results in the opening of either P_1 or P_2, then the short between *VDD* and *GND* is broken. However, this is impossible since all the transistors on both P_1 and P_2 are controlled by signals from other *TGs* (assumption A1), none of which can be controlled by the *TG* containing x and y (assumption A4). Thus a constantly-conducting path from *VDD* to *GND* exists and the bridging fault can be detected by monitoring the current supply.

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If T cannot be found, then there is no input vector which can set x and y to complemented values in the fault-free circuit. Thus for any input vector, x and y are either at the same state (0, 1, or *floating*) or one of them is *floating*. For the former case, the bridging fault is obviously redundant. For the latter, the floating node will be set to the same value as the other node. Since there is no *anomalous reverse conduction* effect in the circuit (assumption A5) and a floating node cannot affect the outputs of a transistor group (assumption A3), this fault cannot affect the logic function of circuit and thus is redundant. □

Case 2 *x and y are in two unrelated transistor groups GX and GY. (Figure 3)*

Lemma 2 *An irredundant single bridging fault satisfying the condition of Case 2 can be detected by using CSM.*

Proof: The proof for this lemma is similar to that for Lemma 1. If an input vector T which sets up P_1 and P_2 as defined in the proof of Lemma 1 can be found, then a conducting path is formed between VDD and GND when T is applied to the faulty circuit. This path cannot be broken due to the voltage redistribution because no control signals to P_1 or P_2 can change as the two *TGs* are unrelated. Thus the fault is detectable using CSM.

If T cannot be found, then by a similar argument as used in Lemma 1, the bridging fault cannot affect the logic function of the circuit and is thus redundant. □

Case 3 *x and y are in two related transistor groups GX and GY. (Figure 4)*

Lemma 3 *An irredundant bridging fault satisfying the condition of Case 3 can be detected by using CSM.*

Proof: Since there is no loop containing GX and GY in the fault-free circuit(assumption A4), only one of them can control the other. Without loss of generalitily, assume GX can

control GY. This assumption does not invalidate the generality of assuming x and y to be set to 1 and 0, respectively, since one can always interchange x with y or GX with GY in the following discussion. Refer to Figure 4. First it must be shown that if an input T which sets x to 1 and y to 0 can be found, then there is a large current consumption in the faulty circuit when T is applied, and thus the fault can be detected. Assume T is found which sets up conducting paths P_1 and P_2 as defined in Lemma 1. When T is applied to the faulty circuit, the bridging fault results in a redistribution of voltage along the path connecting VDD and GND. If this redistribution does not affect any output of GX, or it only affects those outputs of GX which do not affect P_2, then both P_1 and P_2 cannot be broken and a constantly-conducting path exists from VDD to GND. If the redistribution affects some outputs of GX and they in turn affects some transistors on P_2, the following discussion will show that a large current can still be observed. Let O be a set consisting of those output nodes of GX which may affect P_2 due to voltage redistribution. Each element in O must be connected to x through some conducting path, otherwise it cannot be affected by the voltage redistribution. Now if no large current flowing through P_1 ever occurs, P_2 must have been broken due to the voltage redistribution since P_1 cannot be broken. But in this case node x and all nodes in O will charge to their fault-free values since they are all connected to VDD through conducting transistors. This will cause path P_2 to once again become conducting. The result for this is that an oscillation occurs in the faulty circuit. But if oscillation occurs, then at any instant of time there must exist at least one TG which is changing state. Since such a state transition in a CMOS circuit consumes a large current, it is impossible to observe no large current supply flow. Thus it can be concluded that either a large current always flows through P_1 or an oscillation occurs. In both cases, the fault can be detected by using CSM.

If T can not be found, then by the same argument as used in proving Lemma 1, the fault is redundant. □

It is obvious that the above three cases have covered all possible single BFs in the circuits under consideration. Thus the following result can be obtained.

Theorem 1 *A single bridging fault in a combinational circuit is either detected by using CSM or is redundant.*

Example 1: Consider Figure 1. There are three single bridging faults: bf_1, bf_2 and bf_3, belonging to Case 1, Case 2 and Case 3, respectively. By applying (ABCDE)=(10101), all these three BFs are activated. SPICE simulation shows that both bf_1 and bf_2 result in a steady state current flow of 1.64×10^{-4} amperes in the faulty circuit. No oscillation occurs for these two faults. For bf_3, depending on the physical size of transistors, oscillation may or may not occur. When the size of the transistors in the NOR gate are the same as or twice the size of the other transistors in the circuit, no oscillation occurs. The steady state currents for these two cases are 8.2×10^{-5} and 1.7×10^{-4} amperes, respectively. When the size of the transistors in the NOR gate are 3 times the size of the other transistors, oscillation occurs. The current flow for this case is between 0.9×10^{-4} and 2.9×10^{-4} amperes. As expected, in all cases the current values in the faulty circuits are much larger that in the fault-free circuit, which is of the order of nanoamperes.

4   Multiple Bridging Faults

This section considers multiple bridging faults. The following theorem is first proved.

Theorem 2 *If T_1 is a test vector for a single bridging fault f_1, then T_1 is also a test vector for every multiple bridging fault which contains f_1.*

Proof: Refer to Figure 5 where the bridging fault f_1 occurs between x and y. Without loss of generality assume T_1 sets up a conducting path P_1 from VDD to x and a conducting

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path P_2 from GND to y. As described before, if an oscillation occurs in the circuit due to BFs, then the consumed current becomes relatively large and the faults can be detected. Thus only the case where no oscillation occurs need be considered. If during steady state there is no large current flowing through P_1 or P_2, then at least one transistor on P_1 or P_2 must be switched off. Without loss of generality assume transistor t_1 on P_2 is off. Let the input line to t_1 be l_1. l_1 must be an output of another transistor group (assumption A1). Since T_1 sets up P_2 in the faulty-free circuit, it must have set up another path, say P_3, from a power source to l_1 (assumption A3) in the fault-free circuit. Now the value of l_1 has been changed due to faults in the circuit. There are two possible cases for this. If P_3 is not switched off due to some faults other than f_1, then another path, say P_4, from l_1 to an opposite power source must have been formed, and the resulting value of l_1 after voltage redistribution is under the threshold value of t_1. But if this is the case, a conducting path containing P_3 and P_4 from VDD to GND must be formed and a large current flow must exist. Thus the faults is detected. Now consider another case where P_3 has been switched off. For this case to exist, the value of one input, say l_2, to a transistor on P_3 must be the complement of its fault-free value. By a similar argument, either a path, say P_5, set up by T_1 from a power source to l_2 in the fault-free circuit is not cut, but another path, say P_6, from l_2 to an opposite power source is formed, or P_5 is cut. In the former case, the fault is detected. In the latter case, a transistor exists which is on path P_5 and is conducting in the fault-free circuit but non-conducting in the faulty circuit. Continuing this process, since there is no control loops in the fault-free circuit, eventually either a conducting path from VDD to GND is found or a primary input is reached. Recall that a primary input acts as a strong source (assumption A6) and if its value is forced to change, then a large current must flow through that primary input. Thus the faults can be detected. From the above discussion, the theorem follows. □

Corollary 1 follows directly from Theorems 1 and 2.

Corollary 1 *All multiple BFs which contain at least one irredundant single BF are detectable by using CSM, and a test set which detects all single irredundant BFs is sufficient for detecting all such multiple BFs.*

Example 2: Again consider Figure 1. Assume bf_1, bf_2 and bf_3 occur simultaneously. SPICE simulation shows that by applying input vector ABCDE = 10101 to faulty circuits where the size of the transistors in the NOR gate range from one to five times of the size of the other transistors, the steady state current flow remains the same at 3.1×10^{-4} amperes. No oscillation is observed.

5 Conclusion

A systematic analysis on bridging faults in combinational circuits has been given. It has been shown that not only are all irredundant single BFs, but also all multiple BFs which contain at least one irredundant BF are detectable using CSM. More importantly, it has been shown that a test set which detects all irredundant single BFs also detects all mutliple BFs which contain at least one irredundant single BF. Thus the complexity of detecting multiple BFs can be reduced to that of detecting single BFs.

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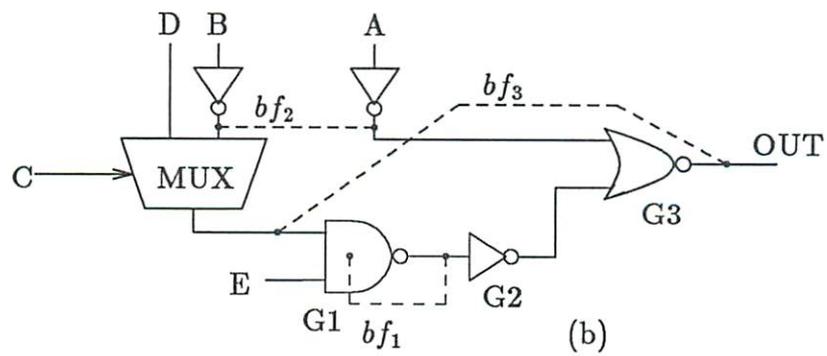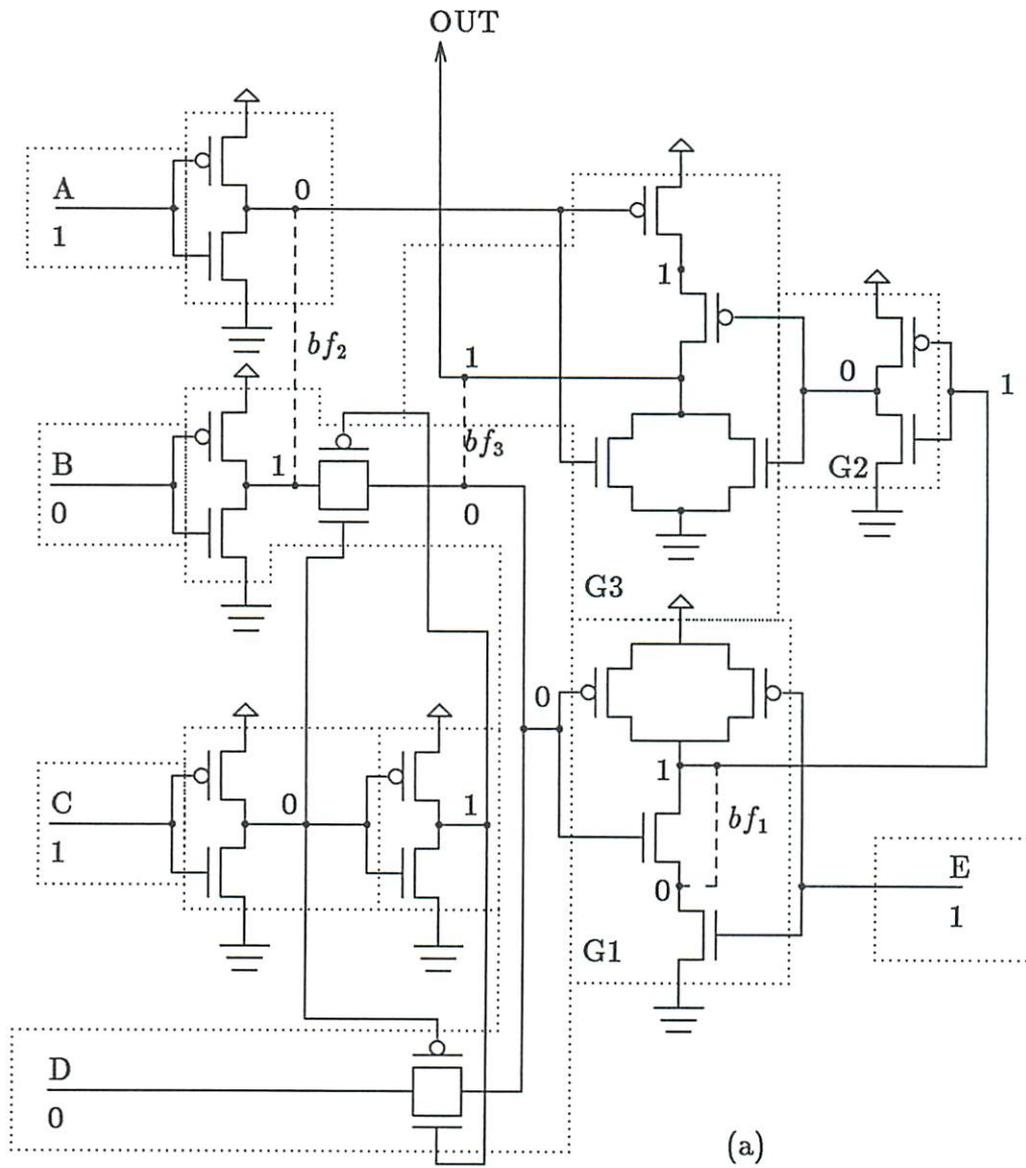
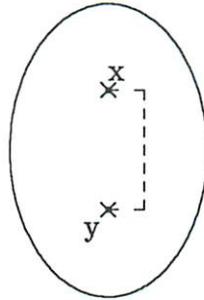Figure 1: Partitioning and BFs of a CMOS circuit

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Figure 2: Case 1: BF inside an *TG*

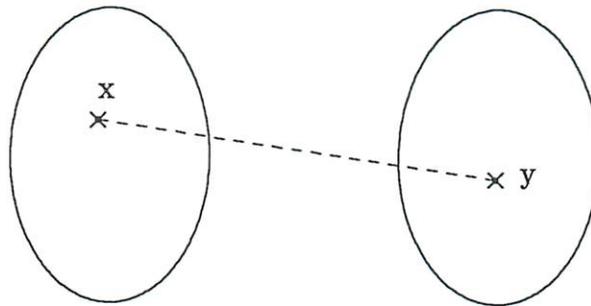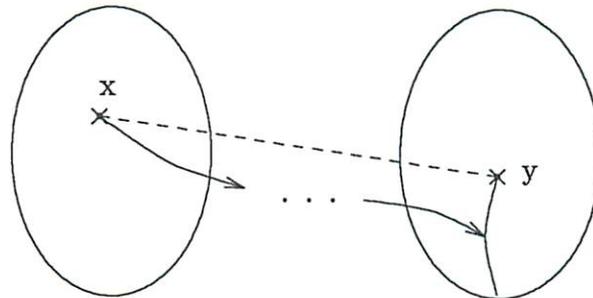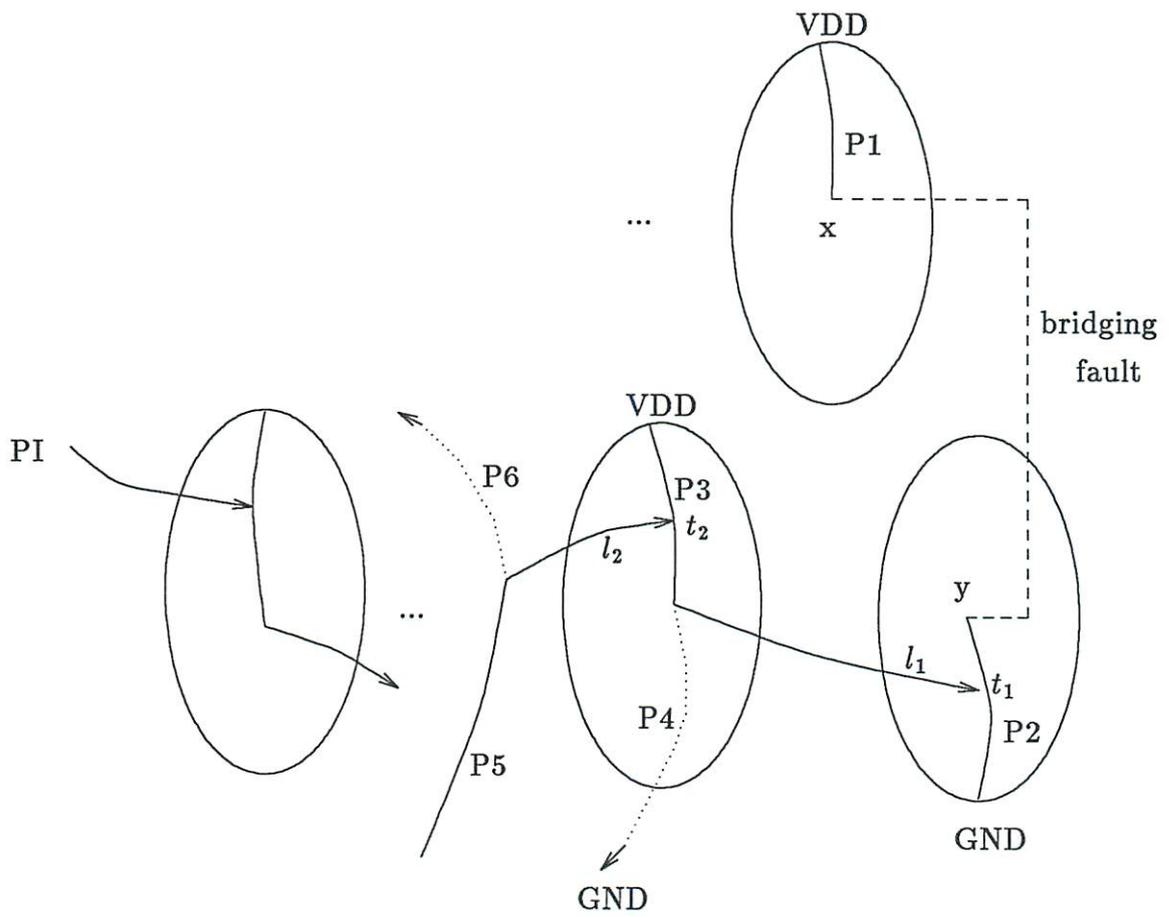Figure 3: Case 2: BF in two unrelated *TGs*

Figure 4: Case 3: BF in two related *TGs*

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Figure 5: Detecting multiple bridging faults