

**Fixed-Node Routing Architecture and  
Its Performance in ATM Networks**

by

*Arthur Y. M. Lin and John A. Silvester*

Technical Report No. CRI 89-26

# Fixed-Node Routing Architecture and Its Performance in ATM Networks

*Arthur Y. M. Lin and John A. Silvester*

Department of Electrical Engineering - Systems  
University of Southern California  
University Park, Los Angeles, CA 90089-0781

## ABSTRACT

The architecture and performance of *fixed-node* virtual channel (VC) routing in ATM networks is studied. In conventional fixed-path routing all packets of a virtual connection, after the call setup phase, follow the same sequence of communication nodes and links. In fixed-node routing, only the nodes are specified and any of the available parallel links between nodes may be used. Applying the fixed-node routing architecture in ATM networks has the advantage of more efficient use of network resources, better availability/reliability as well as performance, and the ability to support super-rate services. The sequencing problem associated with this approach in conventional packet-switched networks is not present in the ATM environment. We analyze the performance of this routing architecture for an internally non-blocking ATM switch with partially shared output buffers based on a discrete-time  $D^{[A]}/D/c/B$  queueing system for general input traffic. The  $D_1 + \dots + D_N/D/c/B$  queueing system is used for periodic traffic models. It is shown that the fixed-node routing architecture yields better performance in terms of delay, loss probability, channel utilization, and switch throughput than its fixed-path counterpart.

# Contents

<b>1</b>	<b>INTRODUCTION</b>	<b>1</b>
<b>2</b>	<b>FIXED-NODE ROUTING ARCHITECTURE</b>	<b>5</b>
<b>3</b>	<b>GENERAL INPUT TRAFFIC</b>	<b>6</b>
3.1	Infinite Buffer . . . . .	6
3.2	Finite Buffer . . . . .	8
3.3	Numerical Results . . . . .	9
<b>4</b>	<b>PERIODIC INPUT TRAFFIC</b>	<b>10</b>
4.1	No Loss System . . . . .	11
4.2	Loss System . . . . .	12
4.3	Numerical Results . . . . .	13
<b>5</b>	<b>CONCLUSIONS</b>	<b>14</b>

# 1 INTRODUCTION

The prevalence of fiber optics and new switching technologies will lead to a new generation of communication system generally called Broadband Integrated Service Digital Network (B-ISDN) which is able to support diverse user demands such as data, voice, graphics, video, images, and their possible combinations in a cost-effective manner. ATM will be the target transfer mode (i.e., multiplexing and switching techniques) solution<sup>1</sup> for implementing B-ISDN [19]. ATM is a specific packet-oriented transfer mode using an asynchronous (statistical) time division multiplexing and switching mechanism, that provides integrated network access as well as an unique basic network transport service. Information is transported in small fixed-length “packets” called *cells*<sup>2</sup> prefixed with a header containing a label that uniquely identifies the virtual channel<sup>3</sup> (VC) over a User-Network Interface (UNI) or Network-Node Interface (NNI). ATM is a connection-oriented technique allowing the network to support both connection-oriented as well as connectionless services [5], [18], [19].

In ATM networks, two adjacent communication nodes (UNI or NNI) are commonly connected by several parallel communication links<sup>4</sup>. Because of the connection-oriented nature of the ATM, two basic approaches exist for routing cells: *fixed-path* and *fixed-node*. Fixed-path routes all cells, during the information transfer phase of a virtual connection (or call), along a fixed sequence of nodes and links while fixed-node specifies only the nodes. The fixed-node routing can be extended by subdividing the channels between any pair of adjacent nodes into a set of *transmission groups* (TG). All succeeding cells after connection setup phase of a call are then moved through a

---

<sup>1</sup>Synchronous Optical Network (SONET) provides the target transmission infra-structure.

<sup>2</sup>Most recently, the size of ATM cell has been standardized by CCITT to have a 48-octet information field plus a 5-octet header.

<sup>3</sup>also called virtual connection, virtual circuit, or virtual link by others.

<sup>4</sup>We use channel and link interchangeably throughout this paper.



predetermined sequence of TGs and nodes [8], [13], [16]. Without loss of the generality, we will focus only on the basic fixed-node scheme in this paper, however.

Applying the fixed-node routing architecture to ATM systems has the advantages of allowing more efficient use of network resources, providing better availability/reliability as well as performance, and supporting super-rate services. The most important feature of ATM is its flexibility in bandwidth allocation and variable user bit-rate support. These can be efficiently exploited by the asynchronous sharing of all resources (switching power, communication channels, and buffer space) between any two adjacent nodes in a network. Information moving through the network is distributed among parallel channels destined to the same next node resulting in more availability/reliability and enhanced performance. A link failure may only lead to a reduced bandwidth between the pair of nodes involved without disrupting existing connections. It will be shown in this paper that the fixed-node routing architecture yields better performance in terms of delay, loss probability, channel utilization, and switch throughput than its fixed-path counterpart. In addition, the fixed-node scheme naturally supports network services with peak rate exceeding the capacity of any single channel - super-rate services.

We analyze the performance of an ATM switch employing the fixed-node routing architecture based on the discrete-time  $D^{[A]}/D/c/B$  queueing system [13]. Stream traffic (e.g. voice, FAX, file transfer) can be modeled as the superposition of a set of periodic arrival processes ( $D_1 + \dots + D_N$ ), while more general traffic can be modeled as a bulk arrival process with constant bulk inter-arrival time and general bulk-size distribution. It is assumed that the time axis is equally divided into time slots (discrete-time) and all arrivals and departures<sup>5</sup> are synchronized with slot boundaries. This assumption is indeed very reasonable due to the synchronous operation of standard-

---

<sup>5</sup>Assume that an arriving cell is transmitted immediately without any delay if there is a free channel.

ized underlying SONET frame [20] and the fixed cell size of ATM. The transmission time of a cell is one time slot. Most of the previous work is for a single-server system [2], [3], [4], [6], [9], [11], [21]. An internally non-blocking ATM switch with *partially* shared output buffers employing the fixed-node routing scheme can be modeled as a multi-server system, however. Both infinite and finite buffer systems (for the case of periodic arrivals, these correspond to no-loss and loss systems respectively) are considered. The resulting queueing system with bulk arrivals, deterministic inter-bulk arrival time ( $D$ ), general bulk-size distribution ( $A$ ), multi-server ( $c$ ), deterministic service ( $D$ ), and buffers of size  $B$  is then generally called the discrete-time  $D^{[A]}/D/c/B$  queueing system. Note that the buffer size  $B$  is defined in this paper as the maximum number of cells *excluding* those in transmission that the system can hold.

Much work has appeared in literature with the majority devoted to the fixed-path routing architecture. Karol, Hluchyj, and Morgan [11] compared the performance of input versus output queueing on a time-slotted space-division fast packet switch. In their analytical model for queues on outputs, they solved the system with infinite buffer and assuming binomial bulk size. Four different approaches for providing the queueing in a high-performance packet switch with finite buffering capacity were later studied by Karol and Hluchyj in [6]. In addition, they considered the problem of using a packet switch for circuit-switched traffic and addressed the tradeoff between the size of buffer required in a switch and the probability that an existing circuit connection is disrupted. Their analysis was based on a discrete-time queueing system with periodic arrival processes. The system was solved by considering all possible arrival patterns (i.e., exhaustive search) [9], [10]. Eckberg and Hou investigated the effects of output buffer sharing on buffer requirements in an ATM packet switch using a discrete-time  $D^{[A]}/D/1$  queueing model with binomial distributed bulk size [4]. In [21], Tran-gia and Ahmadi solved a discrete-time  $G^{[X]}/D/1/S$  (in their terminology) queueing system, motivated by its application in packet-switching systems. Note that for the case of a single-server with finite buffer their analysis is somehow more general



since it incorporates general bulk inter-arrival times. Morris proposed an algorithmic method to analyze a discrete-time  $D/D/1$  queue with infinite as well as finite buffer and applied this approach to packet-switching applications [15]. Recently, efficient recursive computational algorithms were developed by Cidon and Sidi for analyzing the performance of a single-channel ATM system with periodic arrivals.

The concept of routing packets of a virtual circuit<sup>6</sup> based on a multiple link transmission group originally comes from System Network Architecture (SNA) of IBM [7], [8], [14]. A transmission group is a set of parallel (SDLC) links with similar characteristics joining two adjacent nodes. These links can be treated as a single *logical* link that has higher bandwidth and more availability/reliability. Packets of a logical connection are spread over parallel links of any TG along the way to the destination. While enjoying performance and reliability advantages, the fixed-node architecture in conventional packet-switched networks suffers from a resequencing problem caused by variable length packets, and/or different transmission rates associated with different links in a TG<sup>7</sup>. To restore the (end-to-end) ordering of packet transfer for any given connection, a resequencing mechanism is required [1], [24]. This can be implemented on a hop-by-hop and/or an end-to-end basis. However, this problem is not present in ATM networks since the cells are fixed length and it is reasonable to assume that all links in a given TG have the same transmission rate (sequencing problems due to errors are inherent and are properly resolved on an end-to-end basis in ATM networks due to the very low error rates found in optical fibers).

Recently Pattavina [16] considered the problem of bandwidth allocation in a broadband packet switch based on the fixed-node routing scheme (called multichannel bandwidth allocation in his terminology) and showed a feasible hardware implementation in a Batch-banyan switch with input queueing. Some performance results

---

<sup>6</sup>called a virtual route, in SNA's terminology, defined for end-to-end control.

<sup>7</sup>Transmission errors on one of the links may also cause out-of-sequence packet delivery.

obtained using simulation and simplified analysis were also provided. Lai discussed and compared the fixed-node and fixed-path routing schemes in an ISDN offering frame relaying services [12].

The remainder of this paper is organized in the following fashion. In section 2, we address some issues associated with applying the fixed-node routing architecture to ATM networks and compare it with two existing packet network routing approaches. Next, in section 3 and 4, we review the  $D^{[A]}/D/c/B$  and  $D_1 + \dots + D_N/D/c/B$  queueing models of [13] for both general and periodic input traffic assumptions respectively and present some numerical results comparing the fixed-node and fixed-path schemes. Finally, we conclude the paper in section 5.

## 2 FIXED-NODE ROUTING ARCHITECTURE

The emerging demand for various broadband services plus all currently provided packet and circuit services will be integrated through a multimedia ATM BISDN. These potential applications introduce extremely diverse traffic characteristics and raise stringent and very different performance requirements. To provide a guaranteed grade of service for various applications without loss of efficiency, how to route cells through the network must be carefully considered.

Two existing packet network routing architectures are datagram and virtual circuit. Note that our focus is on the network internal architecture rather than the network interface to end users. The datagram mechanism routes each packet independently (i.e., both links and nodes are not fixed). A major advantage of datagram routing is its robustness and flexibility in the face of network component failures; while its main drawback is the lack of effective traffic control and its susceptibility to network congestion. It is also claimed by some that the routing is more difficult



to implement in a high speed network, although this depends on how the routing is implemented. On the other hand, packets of a virtual connection are moved along a fixed sequence of links and nodes across the network by using virtual circuit routing. Compared with datagram, virtual circuit scheme has more control over the information flow (but does not imply an efficient control, however) and reduced per-packet routing overhead but has less robustness and flexibility [25].

As mentioned, ATM is connected-oriented. The fixed-node routing attempts to get the maximum advantage from both existing routing architectures while minimizing their drawbacks. Therefore, the fixed-node VC routing is, in some sense, a hybrid of fixed-path virtual circuit routing and datagram routing. The resource allocation problem including switching power, bandwidth, and buffer space can be solved relatively easily and efficiently by using fixed-node routing. This benefit is due to the pooling effect and the statistical smoothing of a large number of resources corresponding to the set of links between the pair of switch nodes [16].

## 3 GENERAL INPUT TRAFFIC

### 3.1 Infinite Buffer

We shall assume that the input traffic consists of the superposition of  $N$  independent input sources. Cells from a particular source, say  $n$  ( $1 \leq n \leq N$ ), arrive at the system (a tagged queue under consideration for links destined to the same next node in an ATM switch) according to a random process<sup>8</sup>

$$\mathbf{A}^{(n)} = \{A_i^{(n)} : 1 \leq i < \infty\}$$

---

<sup>8</sup>Here we adopt the convention of using subscripts to indicate evolution in time and superscripts to indicate the particular source.

where  $A_i^{(n)}$  is the r.v. of the number of arrivals to the system at the beginning of time slot  $i$  from source  $n$ . For any  $n$  ( $1 \leq n \leq N$ ), the random variables  $\{A_i^{(n)} : 1 \leq i < \infty\}$  are assumed to be independent and identically distributed (i.i.d.) with known pmf  $a_i^{(n)}(k) \triangleq P[A_i^{(n)} = k] = a^{(n)}(k)$  and have finite mean,  $\lambda^{(n)} = E[A_i^{(n)}]$ , and variance,  $\sigma_{A_i^{(n)}}^2 = Var(A_i^{(n)})$ . The overall input process to the system can thus be modeled as a bulk (or batch) arrival process with deterministic bulk inter-arrival time (i.a.t.) equaling to one slot and general bulk-size distribution  $\{A_i : 1 \leq i < \infty\}$ . The total number of cells arriving to the system at the beginning of slot  $i$  is given by

$$A_i = A_i^{(1)} + A_i^{(2)} + \dots + A_i^{(N)}$$

Again the random variables  $\{A_i : 1 \leq i < \infty\}$  are also i.i.d. with pmf  $a_i(k) \triangleq P[A_i = k] = a(k)$  and its corresponding probability generating function (p.g.f.)  $A(z)$  and have finite mean,  $\lambda = E[A_i]$  and variance,  $\sigma_{A_i}^2 = Var(A_i)$ .

Let  $Q$  be the r.v. of the number of cells waiting in the queue (i.e., the backlog) at steady (equilibrium) state. Adopting the results of [13], we then have the mean and variance of the queue size:

$$\bar{Q} = \frac{A''(1) - c(c-1)}{2(c-\lambda)} + \sum_{m=1}^{c-1} \frac{1}{1-\theta_m} \quad (1)$$

$$\begin{aligned} \sigma_Q^2 &= \left\{ \frac{2}{3} + \frac{2[A''(1) - c(c-1)]}{c-\lambda} \right\} \sum_{m=1}^{c-1} \frac{1}{1-\theta_m} \\ &+ \frac{A'''(1) - c(c-1)(c-2)}{3(c-\lambda)} + \frac{[A''(1) - c(c-1)]^2}{2(c-\lambda)^2} + \bar{Q} - (\bar{Q})^2 \end{aligned} \quad (2)$$

where

$$A''(1) = \left. \frac{d^2 A(z)}{dz^2} \right|_{z=1} = E[A_i^2]$$

$$A'''(1) = \left. \frac{d^3 A(z)}{dz^3} \right|_{z=1} = E[A_i^3]$$

and  $\theta_m (m = 1, \dots, c-1)$  are the  $c-1$  complex zeros of the equation

$$z^c - A(z) = 0$$

inside  $|z| \leq 1$  while the  $c^{\text{th}}$  is clearly  $z = 1$  (i.e.,  $\theta_c = 1$ ) [13].

Example: fixed-path routing with binomial bulk size

Now, considering a fixed-path routing ( $c=1$ ) system,  $Q(z)$  becomes

$$Q(z) = \frac{(1-\lambda)(z-1)}{z-A(z)}$$

If  $A_i$  has the binomial pmf

$$a(k) = P[A_i = k] = \binom{N}{k} p^k (1-p+pz)^{N-k} \quad 0 \leq k \leq N$$

and its corresponding p.g.f.

$$A(z) = (1-p+pz)^N$$

where  $p (= \lambda)$  is the probability that a cell will arrive at the system from any source in any given time slot. After some algebra, we find the mean and variance of queue size for  $c = 1$  case from (1) and (2) as follows:

$$\bar{Q} = \frac{N(N-1)p^2}{2(1-p)} \quad (3)$$

$$\sigma_Q^2 = \frac{N(N-1)(N-2)p^3}{3(1-p)} + \frac{N(N-1)p^2}{2(1-p)} + \frac{[N(N-1)]^2 p^4}{4(1-p)^2} \quad (4)$$

These are identical to the results in [4] and [11].

### 3.2 Finite Buffer

In this subsection, we consider the same queueing system except the buffer space is now assumed to be finite with size  $B$  ( $B < N - c$ ). In this case we are most interested in the probability of cell loss,  $\phi$ , we use the result of [13],

$$\phi = \frac{1}{\lambda} \sum_{k=0}^B q(k) \sum_{n=B+c+1-k}^N (n+k-B-c) \cdot a(n) \quad (5)$$



where  $q(k)$  is the steady state queue size distribution for this finite buffer system. The system is solved by a numerical technique [13], [17]. The (effective) waiting time,  $\bar{W}^*$ , averaged over cells admitted into the queue is given by

$$\bar{W}^* = \frac{\bar{Q}}{\lambda^*}$$

where

$$\lambda^* = \lambda(1 - \phi)$$

$\lambda^*$  is the effective input rate of the system defined as the rate of cells actually entering the system. For the case of fixed-path routing ( $c=1$ ), the results presented here correspond to the result in [6].

### 3.3 Numerical Results

We demonstrate some numerical examples for various performance measures of interest in this subsection. The system model of an  $N$  by  $N$  internally non-blocking ATM switch with partially shared output buffer applying the fixed-node routing architecture is shown in figure 1. Assume uniform input and output traffics while the imbalance traffic case is currently under study. For simplicity of presentation, we use a binomial distributed bulk-size for the input traffic<sup>9</sup>. Each input port generates a cell in any time slot with probability  $p$  (i.e., offered load). Figure 2 shows the average waiting time as a function of the offered load per input port under the infinite buffer assumption for fixed-path routing corresponding to the  $c = 1$  case and fixed-node routing with different numbers of channels,  $c$ , between a pair of nodes. The waiting time is dramatically reduced as  $c$  increases. For the finite buffer case, we compare the fixed-path ( $c = 1$ ) approach with the fixed-node approach for a system with 8 channels ( $c = 8$ ). We present results for the waiting time and loss probability for various

---

<sup>9</sup>More general bulk-size distribution and the effects of traffic burstiness can also be taken in account without much difficulty.

comparable buffer sizes for a switch of size  $N = 40$ <sup>10</sup>. Again, the performance advantage favoring the fixed-node routing is clearly shown in both performance measures in figures 3 and 4, respectively. In addition, in figure 5, we plot the loss probability for several cases in which the buffer size is twice the number of channels to exhibit the fact that the larger the number of channels, the greater the performance improvement. Figures 6 and 7 show the loss probability as a function of the buffer size and the switch size, individually, for the fixed-path ( $c = 1$ ) as well as the fixed-node with 4 channels ( $c = 4$ ) under the offered load generated by  $p = 0.6$  and  $p = 0.8$ . The loss probability is plotted against buffer size under several loading conditions varying from 0.6 to 0.9 for the two routing schemes by having the fixed-node one with 4 ( $c = 4$ ) and 8 ( $c = 8$ ) channels, respectively, on a 32 by 32 switch in figures 8 and 9. All these results consistently show that the fixed-node routing architecture outperforms its fixed-path counterpart. The performance improvement is greater when the number of parallel channels between a pair of adjacent network nodes is larger.

## 4 PERIODIC INPUT TRAFFIC

In this section, we consider the same queueing system but with periodic input process which can then be modeled as a discrete-time  $D_1 + \dots + D_N/D/c/B$  queueing system. An efficient computational algorithm for analyzing the performance of the queueing system is presented by extending the methods developed in [2] to multiple channels. Only results are shown here. For details, the reader can refer to [13].

---

<sup>10</sup>Here, we assume the switching node under consideration is connected to five neighboring nodes with eight channels each. Similar arguments apply to all configurations presented in this paper for the sake of simplicity.

## 4.1 No Loss System

A *frame* is defined to be any  $F$  consecutive time slots. The input process consists of  $N$  ( $D_1, \dots, D_N$ ) independent periodic input sources and each source generates exactly one arrival per frame. For a stable system, the obvious condition  $N \leq c \cdot F$  must hold. In this subsection, the system is assumed to be capable of storing  $N - c$  cells (excluding those cells in transmission) to guarantee no loss. For a given set of input sources, the  $N$  cells arrive in an unique pattern [2], [9]. It is assumed that the  $N$  arriving cells are uniformly distributed over a frame of length  $F$ . Let  $a_{F,N}(k)$  be the probability that  $k$  out of the  $N$  cells arrive at the beginning of any slot in a frame of size  $F$  and  $q_{F,N}(k)$  be the probability that a typical slot in the system has a queue size of  $k$ . We thus have

$$a_{F,N}(k) = \binom{N}{k} \left(\frac{1}{F}\right)^k \left(1 - \frac{1}{F}\right)^{N-k} \quad 0 \leq k \leq N \quad (6)$$

The set of recursive computational equations for calculating the queue size pmf of a no-loss  $D_1 + \dots + D_N/D/c/B$  queueing system is then given by [13]

$$q_{F,0}(k) = 0 \quad F \geq 1, k \geq 1 \quad (7)$$

$$q_{F,N}(k) = 0 \quad F \geq 2, k \geq 1, 1 \leq N \leq k \quad (8)$$

$$q_{1,N}(k) = \begin{cases} 1 & k = N - c, N > c \\ 1 & k = 0, 0 \leq N \leq c \\ 0 & \text{otherwise} \end{cases} \quad (9)$$

$$q_{F,N}(k) = \begin{cases} 1 & k = 0, N \leq c \\ 0 & k \neq 0, N \leq c \end{cases} \quad (10)$$

$$q_{F,N}(0) = \sum_{n=0}^c a_{F,N}(n) \left[ \sum_{k=0}^{c-n} q_{F-1,N-n}(k) \right] \quad F \geq 2, N \geq c \quad (11)$$

$$q_{F,N}(k) = \sum_{n=0}^{k+c} a_{F,N}(n) q_{F-1,N-n}(k-n+c) \quad F \geq 2, 1 \leq k \leq N - c \quad (12)$$



Note that  $q_{F,N}(k) = 0$  whenever  $N > c \cdot F$ . Now the average queue size,  $\bar{Q}_{F,N}$ , is simply

$$\begin{aligned}\bar{Q}_{F,N} &= \sum_{k=1}^{N-c} k q_{F,N}(k) \\ &= \sum_{n=0}^N a_{F,N}(n) \bar{Q}_{F-1,N-n} + \frac{F}{N} - c + c \left[ \sum_{n=0}^{c-1} a_{F,N}(n) \sum_{k=0}^{c-n-1} q_{F-1,N-n}(k) \right] \quad (13)\end{aligned}$$

We can apply Little's result to obtain the average waiting time in the queue,  $\bar{W}_{F,N}$ , as

$$\bar{W}_{F,N} = \frac{F}{N} \bar{Q}_{F,N}$$

The pmf of the waiting time,  $W_{F,N}(k)$ , of a typical cell can also be found as follows:

$$W_{F,N}(k) = \sum_{N_1=0}^{N-1} \frac{a_{F,N}(N_1)}{N_1 + 1} \sum_{N_2=0}^{N_1} \sum_{l=kc-N_2}^{(k+1)c-1-N_2} q_{F-1,N-N_1-1}(l) \quad (14)$$

## 4.2 Loss System

We now proceed to consider the case of a loss system in which the maximum number of cells (excluding those cells in transmission),  $B$  (buffer size), that may be stored is less than  $N - c$ . When an arriving cell from a particular source is lost, all cells from this source will be lost [22], [23]. In this paper, we are interested in determining the loss probability,  $\phi_{F,N}$ , of a typical cell for a specific set of input sources.

The analysis of the loss system follows the same procedure as the no-loss system presented in last subsection except equation (9) becomes

$$q_{1,N}(k) = \begin{cases} 1 & k = 0, 0 \leq N \leq c \\ 1 & k = N - c, c \leq N \leq c + B \\ 1 & k = B, N \geq c + B \\ 0 & \text{otherwise} \end{cases} \quad (15)$$

and equation (12) is still valid for  $k < B$ . In addition, we have

$$\begin{aligned} q_{F,N}(B) &= 0 \quad F \geq 2, N \leq c + B \\ q_{F,N}(B) &= \sum_{n=c}^{B+c-1} a_{F,N}(n) q_{F-1,N-n}(B+c-n) + \sum_{n=B+c}^N a_{F,N}(n) \quad F \geq 2 \end{aligned} \quad (16)$$

We are now in a position to evaluate the loss probability,  $\phi_{F,N}$ , as follows:

$$\phi_{F,N} = \sum_{l=0}^B \sum_{n=l+c}^{N-1} \frac{(n+1-l-c)a_{F,N-1}(n)}{n+1} q_{F-1,N-n-1}(B-l) \quad (17)$$

The effective arrival rate,  $\lambda^*$ , is thus

$$\begin{aligned} \lambda^* &= \lambda(1 - \phi_{F,N}) \\ &= \frac{N}{F}(1 - \phi_{F,N}) \end{aligned}$$

So the average waiting time in the queue,  $\bar{W}_{F,N}^*$ , averaged over those cells admitted into the system is given by:

$$\bar{W}_{F,N}^* = \frac{\bar{Q}_{F,N}}{\lambda^*}$$

where

$$\bar{Q}_{F,N} = \sum_{k=1}^B k \cdot q_{F,N}(k)$$

### 4.3 Numerical Results

For the periodic input traffic, figure 10 and 11 show the waiting time and the cell loss probability, respectively, as a function of the normalized buffer size  $B$  (defined as the average size of buffers per channel) for a fixed frame size,  $F = 10$ , and various  $c$  under the same loading condition (80%). Note that in figure 10 the waiting time become fixed and there is no loss for  $B > N - c$ . We find the similar performance advantages as in the non-periodic input traffic case. For a given loss probability, the buffer size required in fixed-node routing approach is less than in fixed-path approach.

## 5 CONCLUSIONS

In this paper, we study the performance of an ATM switch applying a fixed-node routing architecture based on the discrete-time  $D^{[A]}/D/c/B$  queueing model and compare its performance to the more common fixed-path approach. We present results for both random and periodic arrival processes for both finite (loss system) and infinite (no loss system) buffer assumptions. The results study delay and loss probability as a function of loading, number of channels, switch size (i.e., number of sources), and buffer size.

As indicated and quantified in [6] and [11], both output queueing and completely shared buffering achieve the optimal delay-throughput performance in an ATM switch with fixed-path routing because cells are delayed or lost only when two or more cells from different inputs simultaneously arrive at the same output. This delay and/or loss probability can be further reduced by using the proposed fixed-node routing in an ATM switch with partially shared output buffers, especially under the condition of (transient) imbalanced input and/or output traffic. The performance improvements gained by employing the fixed-node approach are shown by means of various numerical examples. The fixed-node routing concept provides additional advantages of super-rate services, better link reliability/availability, less total buffer requirement, and efficient bandwidth allocation.



## References

- [1] F. Baccelli and A. M. Makowski. "Queueing models for systems with synchronization constraints". *Proc. of the IEEE*, vol. 77, no. 1, pp. 138-161, Jan. 1989.
- [2] I. Cidon and M. Sidi. "Performance analysis of asynchronous transfer mode (ATM) systems". Technical report, RC-14395 (#64197), IBM Research Division, T. J. Watson Research Center, Yorktown Heights, N.Y., Jan. 17 1989.
- [3] A. E. Eckberg. "The single server queue with periodic arrival process and deterministic service times". *IEEE Trans. Commun.*, vol. COM-27, no. 3, pp. 556-562, March 1979.
- [4] A. E. Eckberg and T.-C. Hou. "Effects of output buffer sharing on buffer requirements in an ATDM packet switch". In *Proc. IEEE INFOCOM '88*, pp. 459-466, 1988.
- [5] P. Gonet, P. Adam, and J. P. Coudreuse. "Asynchronous time-division switching: the way to flexible broadband communication networks". In *Proc. Int. Zurich Semi. Digit. Commun. '86*, pp. 141-148, 1986.
- [6] M. G. Hluchyj and M. J. Karol. "Queueing in high-performance packet switching". *IEEE J. Select. Areas Commun.*, vol. SAC-6, no. 9, pp. 1587-1597, Dec. 1988.
- [7] W.N. Hsieh and I. Gitman. "Routing strategies in computer networks". *IEEE Comput. Mag.*, vol. 17, no. 6, pp. 46-56, June 1984.
- [8] J. M. Jaffe, F. H. Moss, and R. A. Weingarten. "SNA routing: past, present, and possible future". *IBM Syst. J.*, vol. 22, no. 4, pp. 417-434, 1983.
- [9] M. J. Karol and M. G. Hluchyj. "Using a packet switch for circuit-switched traffic: a queueing systems with periodic input traffic". *IEEE Trans. Commun.*, vol. COM-37, no. 6, pp. 623-625, June 1989.
- [10] M. J. Karol and M. G. Hluchyj. "Using a packet switch for circuit-switched traffic: a queueing systems with periodic input traffic". In *Proc. ICC '87*, pp. 1677-1682, 1987.
- [11] M. J. Karol, M. G. Hluchyj, and S. P. Morgan. "Input versus output queueing on a space-division packet switch". *IEEE Trans. Commun.*, vol. COM-35, no. 12, pp. 1347-1356, Dec. 1987.
- [12] W. S. Lai. "Network and nodal architectures for the internetworking between frame relaying services". *ACM Comput. Commun. Review*, vol. 19, no. 1, pp.72-84, Jan. 1989.

- [13] Arthur Y. M. Lin and John A. Silvester. "Queueing analysis of an ATM switch with multi-channel transmission groups". Technical report, CRI-89-25, Networks and Distributed Systems Laboratory, Dept. of EE-Systems, Univ. of Southern California, Sept. 1989.
- [14] J. Martin. "*SNA: IBM's Networking Solution*". Prentice Hall, Englewood Cliffs, NJ, 1987.
- [15] R. J. T. Morris. "An algorithmic technique for a class of queueing models with packet switching applications". In *Proc. ICC '81*, pp. 41.2.1-41.2.6, 1981.
- [16] A. Pattavina. "Multichannel bandwidth allocation in a broadband packet switch". *IEEE J. Select. Areas Commun.*, vol. SAC-6, no. 9, pp. 1489-1499, Dec. 1988.
- [17] W. H. Press, B. P. Flannery, S. A. Teukolsky, and W. T. Vetterling. "*Numerical recipes in C: the art of scientific computing*". Cambridge University Press, Cambridge, 1988.
- [18] M. D. Prycker. "Definition of network options for the Belgian ATM broadband experiment". *IEEE J. Select. Areas Commun.*, vol. SAC-6, no. 9, pp. 1538-1544, Dec. 1988.
- [19] T1S1 Technical Sub-Committee. "Broadband aspects of ISDN". Working Draft, May 1989.
- [20] ANSI T1.105-1988. "American National Standard for Telecommunications: Digital Hierarchy - Optical Interface Rates and Formats Specification". March 1988.
- [21] P. Tran-gia and H. Ahmadi. "Analysis of a discrete-time  $G^{[X]}/D/1 - S$  queueing system with applications in packet-switching systems". In *Proc. IEEE INFO-COM '88*, pp. 861-870, 1988.
- [22] C. Yuan. "*On the performance of protocols to support integrated voice and data services*". PhD thesis, Dept. of Electrical Engineering - Systems, Univ. of Southern California, Dec. 1988.
- [23] C. Yuan and J. A. Silvester. "Queueing analysis of delay constrained voice traffic in a packet switching system". *IEEE J. Select. Areas Commun.*, vol. SAC-7, no. 5, pp. 729-738, June 1989.
- [24] T.-S. P. Yum and T.-Y. Nagi. "Resequencing of messages in communication networks". *IEEE Trans. Commun.*, vol. COM-34, no. 2, pp. 143-149, Feb. 1986.
- [25] Lixia Zhang. "Some thoughts on the packet network architecture". *ACM Comput. Commun. Review*, vol. 17, no. 1 & 2, pp. 3-17, Jan./Apr. 1987.

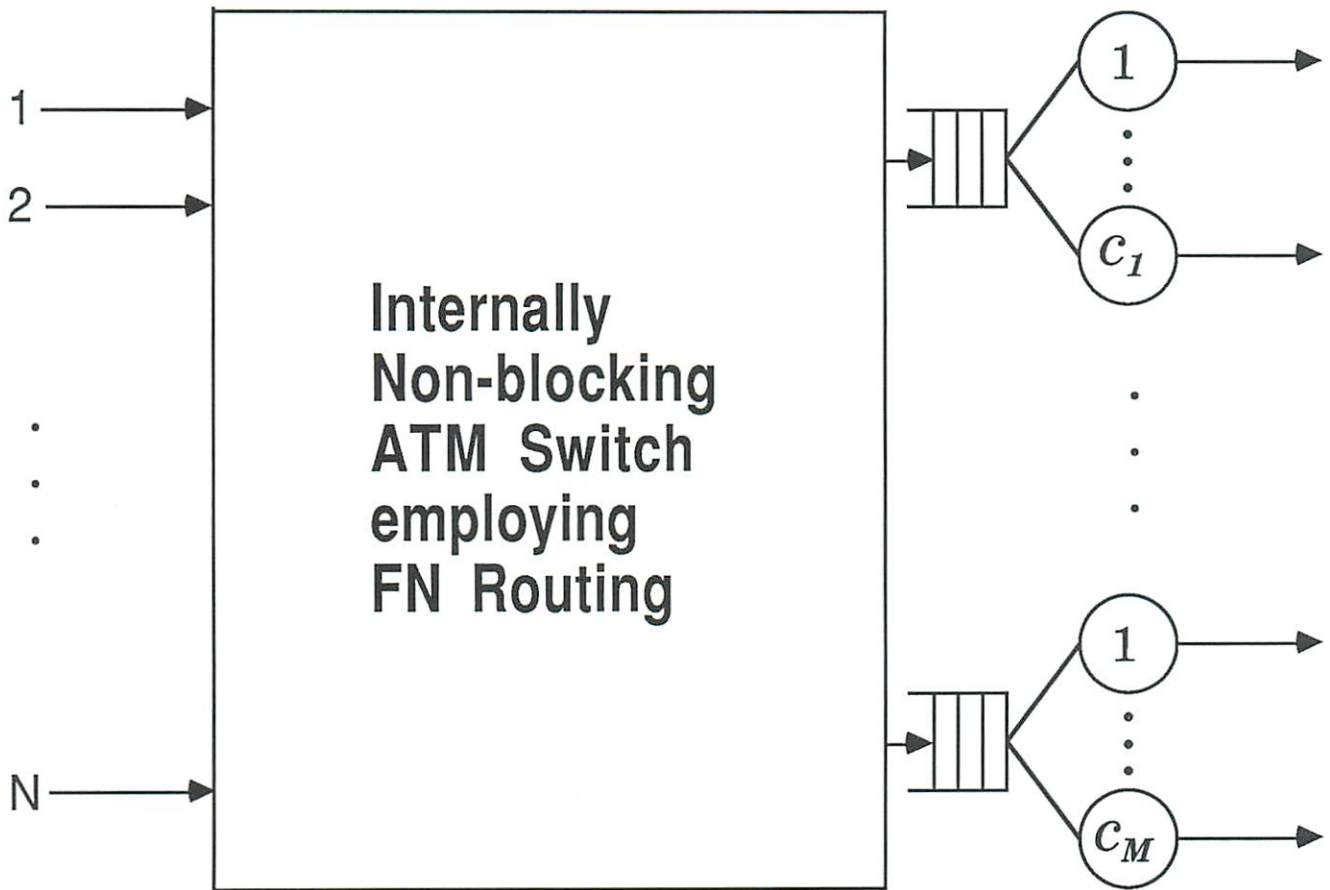


Fig. 1: The system model of an internally nonblocking ATM switch employing fixed-node (FN) routing architecture.



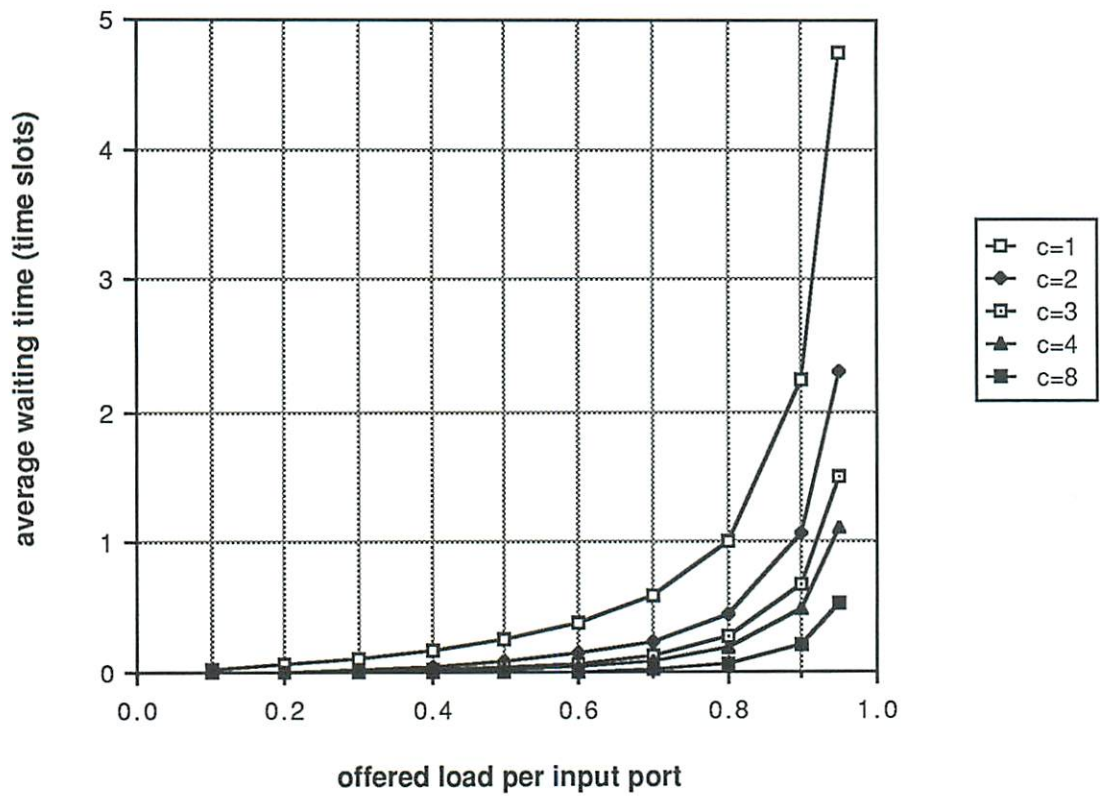


Fig. 2: The average waiting time for various  $c$  and infinite buffer case.

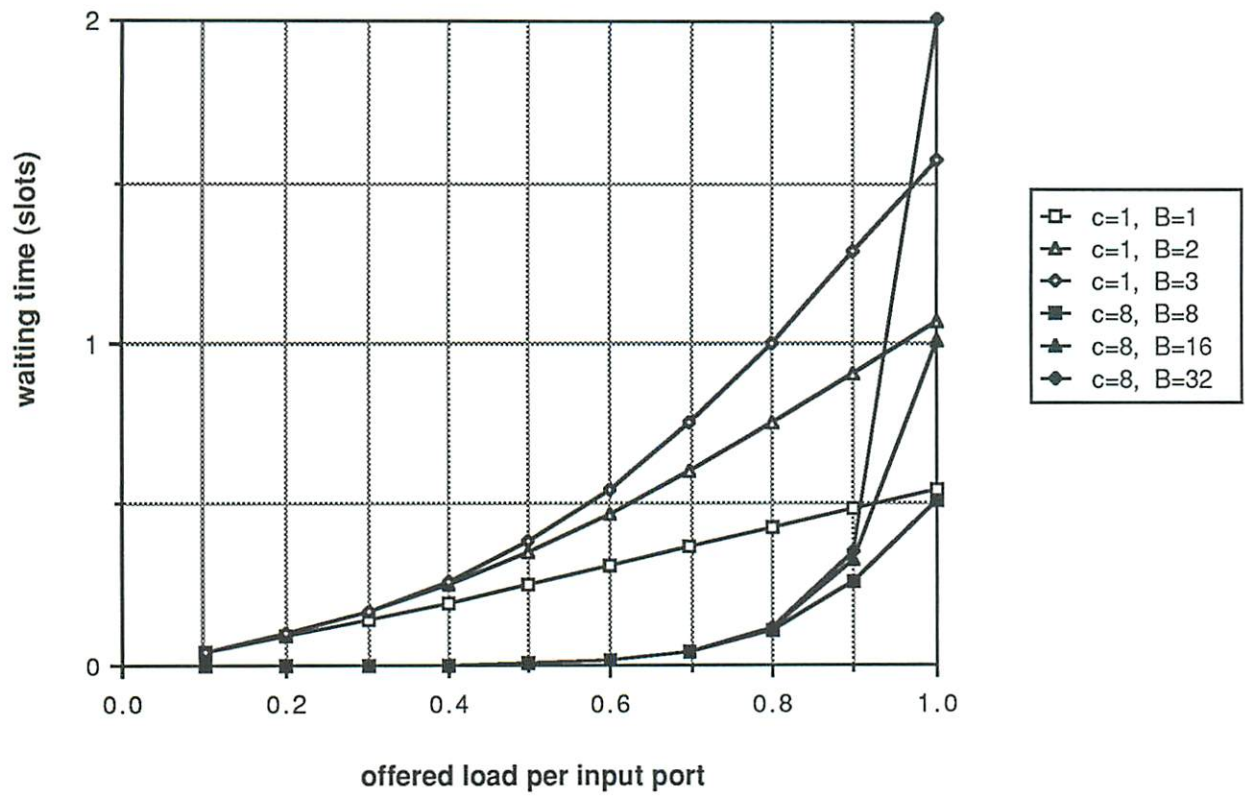


Fig. 3: The waiting time for  $c=1$  and  $c=8$ , and various  $B$  and  $N=40$ .

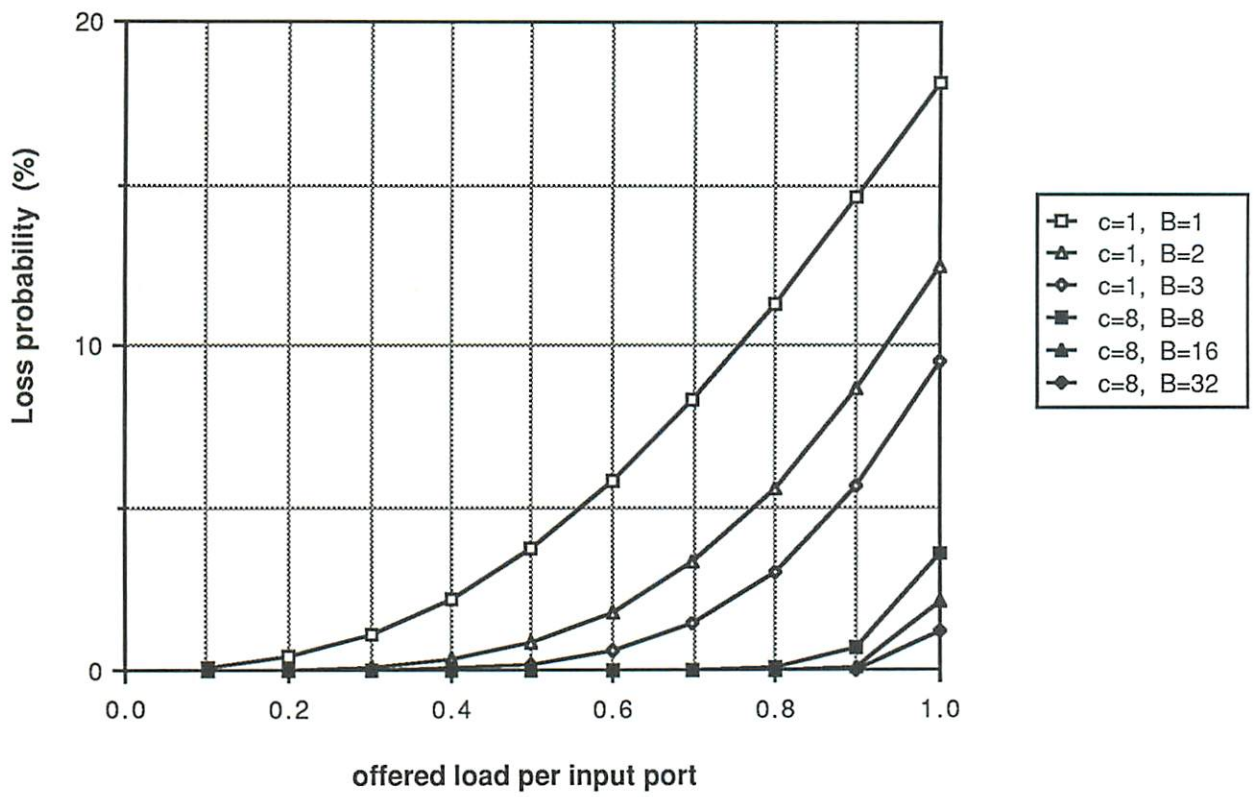


Fig. 4: The loss probability for  $c=1$  and  $c=8$ , and various  $B$  and  $N=40$ .



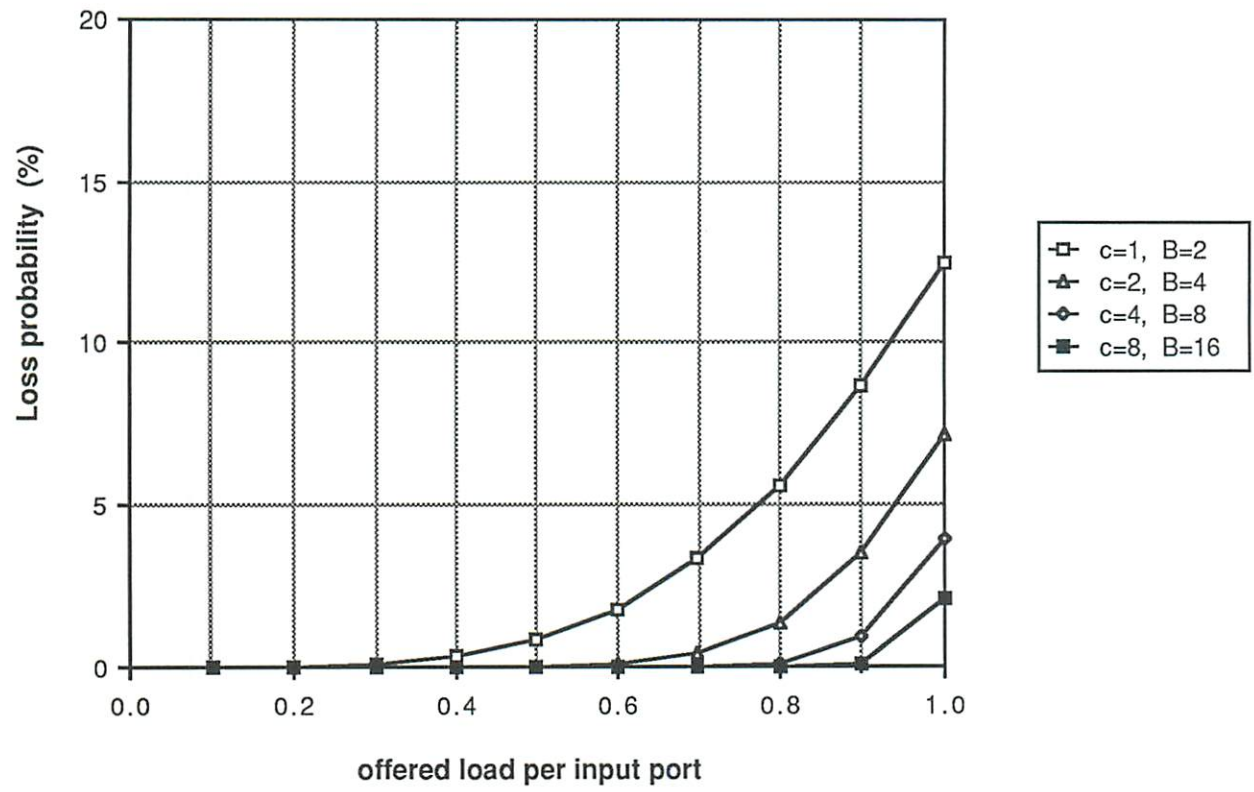


Fig. 5: The loss probability for various cases of  $B=2c$  and  $N=40$ .

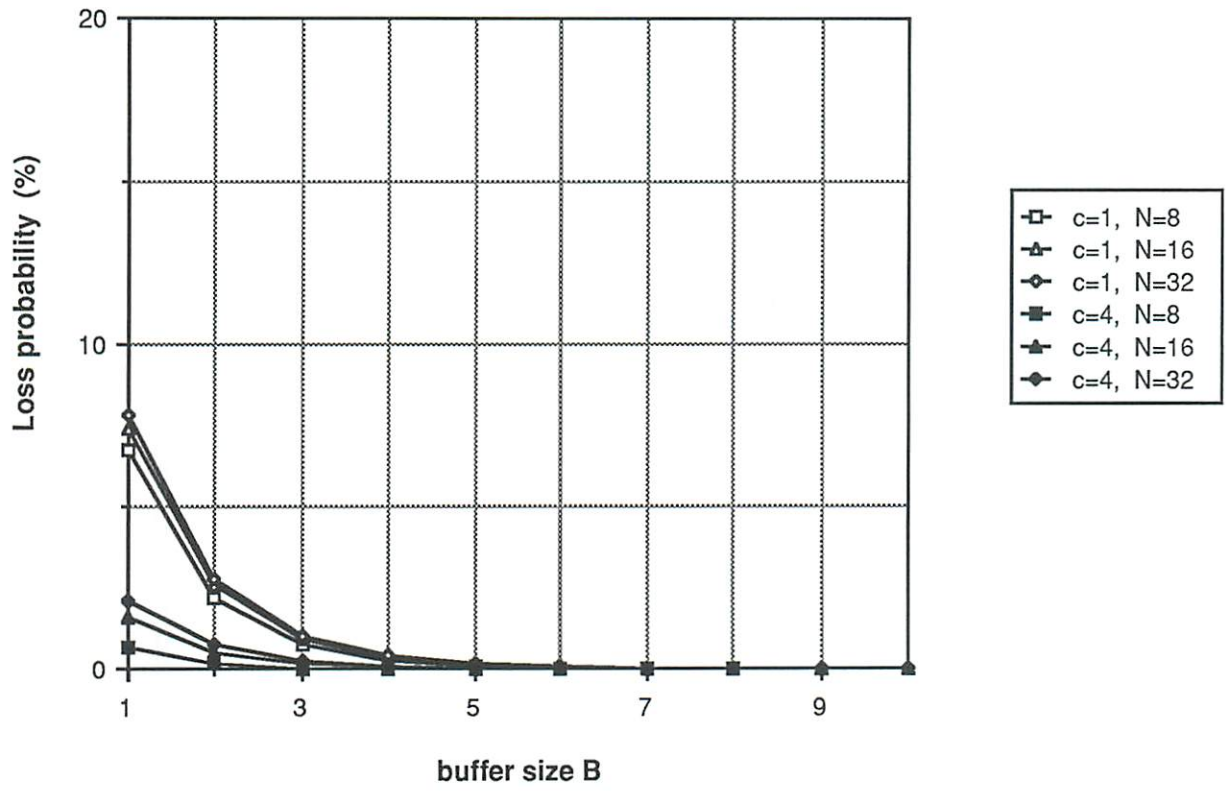


Fig. 6: The loss probability as a function of B and N, for  $c=1,4$  and  $p=0.6$ .

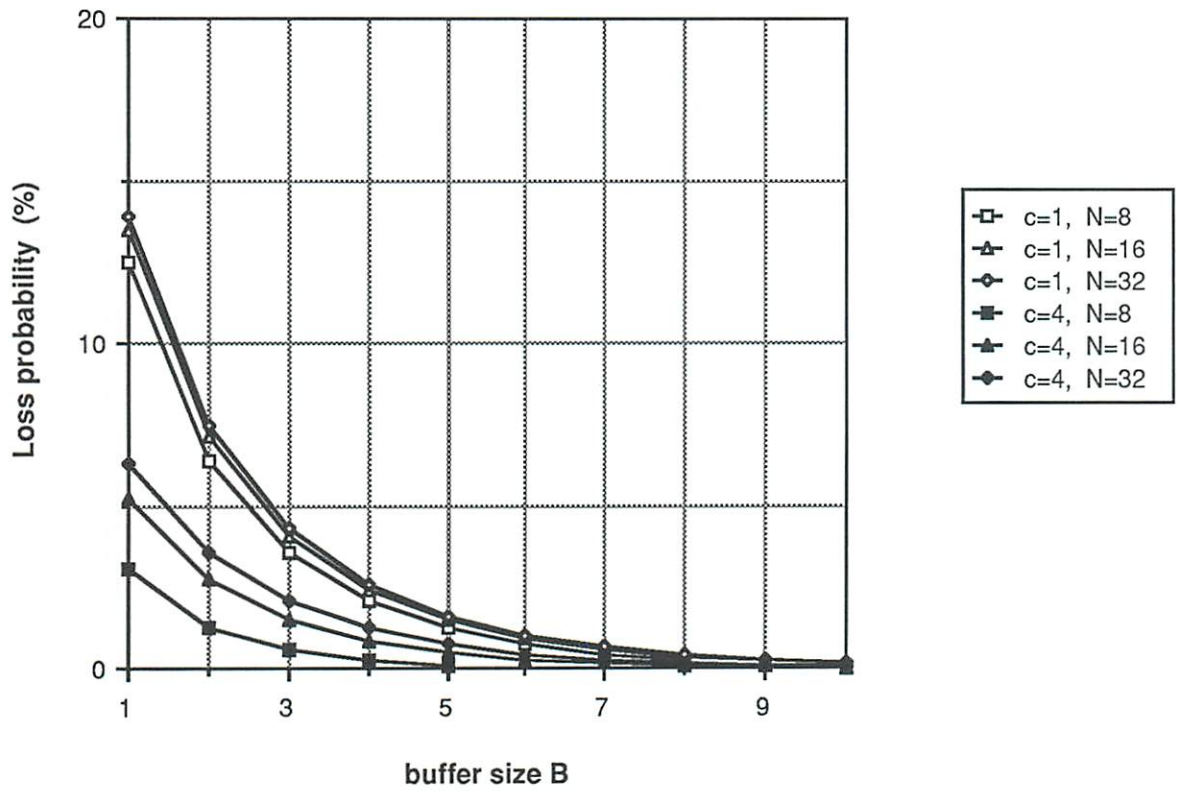


Fig. 7: The loss probability as a function of B and N, for c=1,4 and p=0.8.



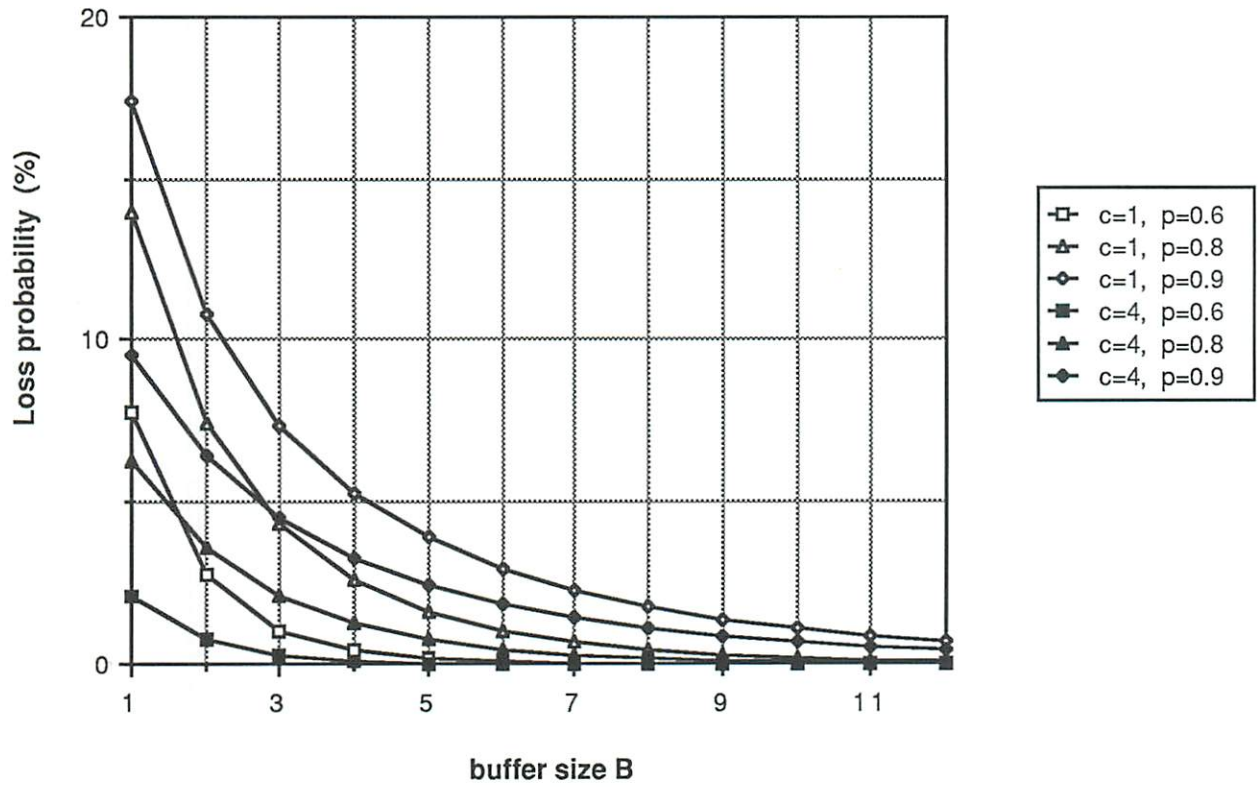


Fig. 8: The loss probability as a function of B and p, for c=1,4 and N=32.

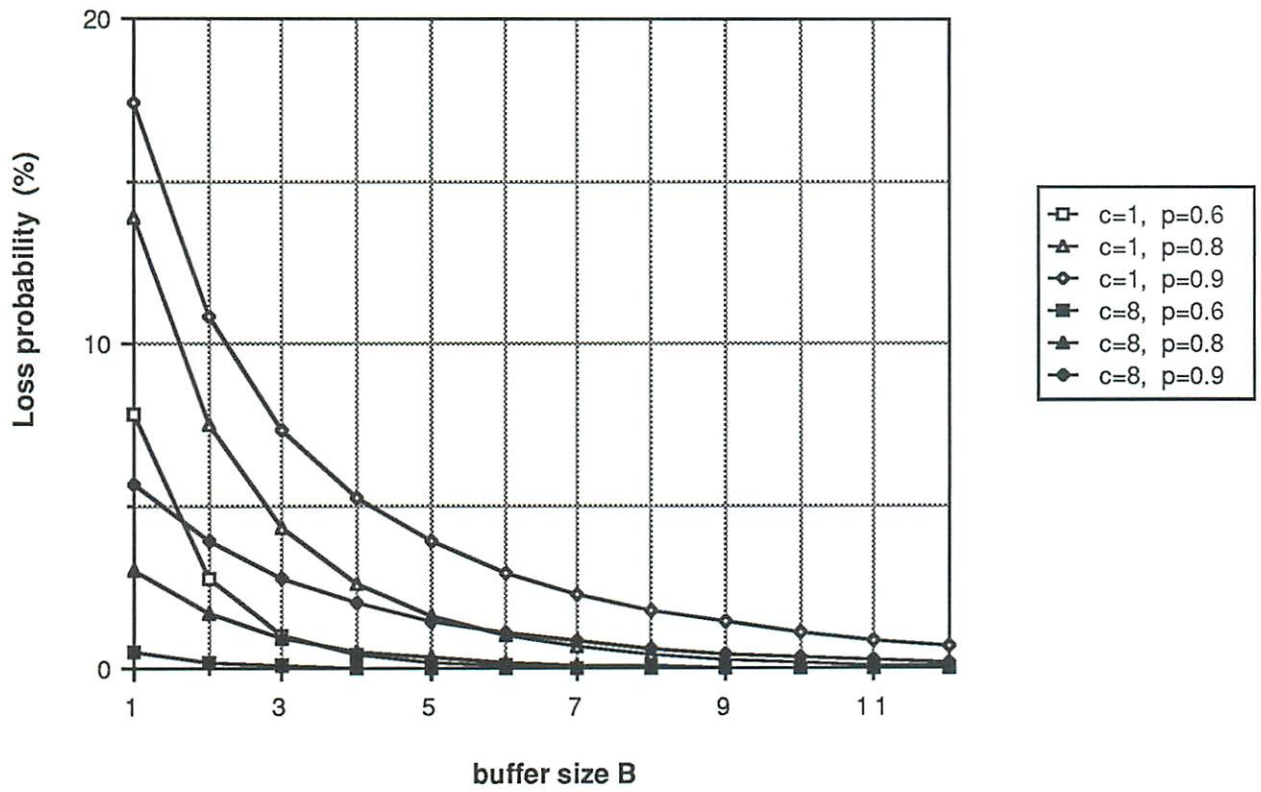


Fig. 9: The loss probability as a function of B and p, for c=1,8 and N=32.

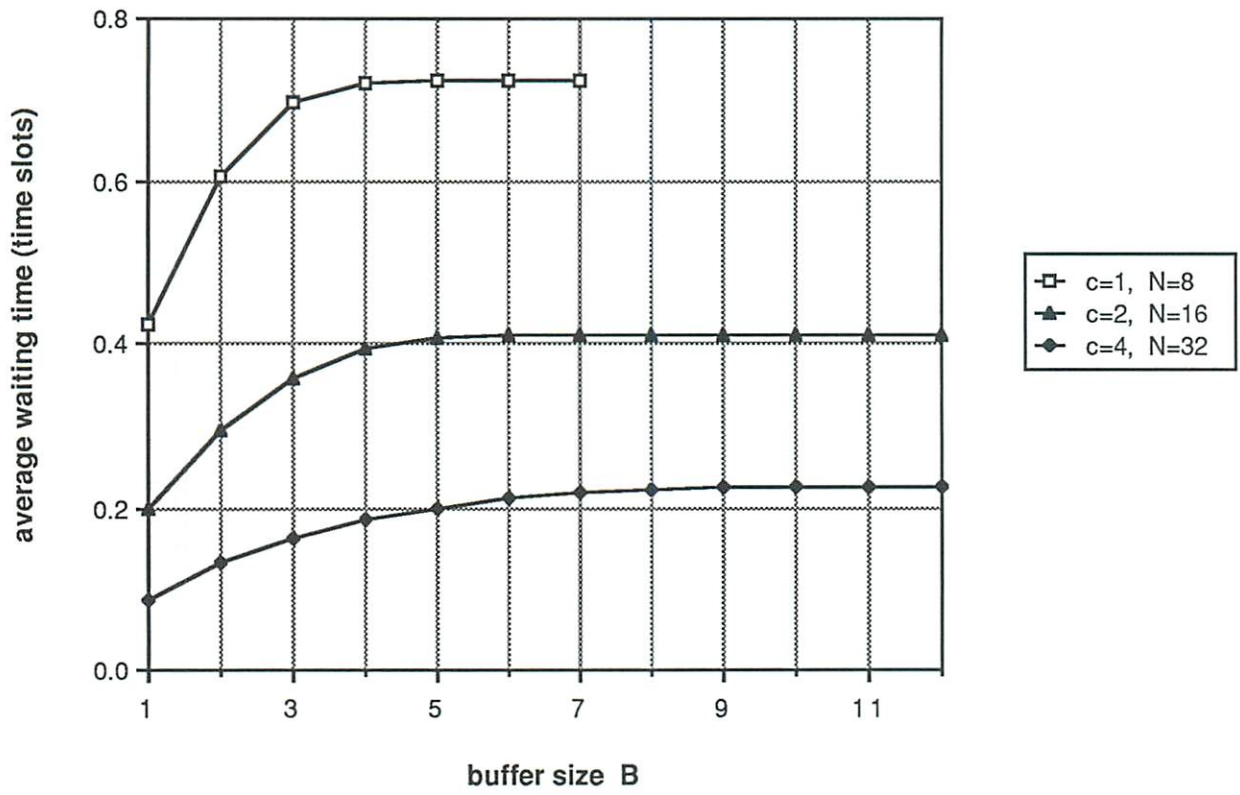


Fig. 10: The average waiting time as a function of B for F=10 and various c.



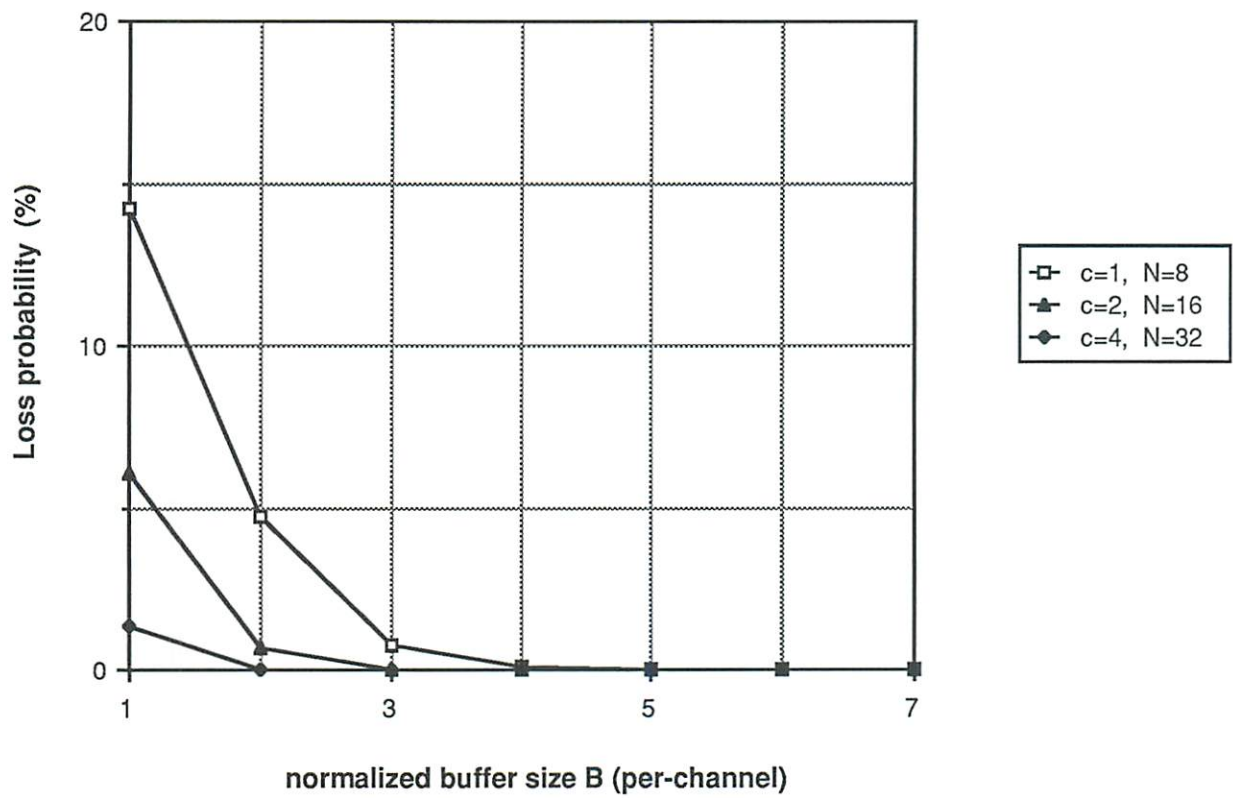


Fig. 11: The loss probability as a function of normalized B for  $F=10$  and various  $c$ .