Stochastic Testability Analysis in Homogeneous Circuits

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Abstract

In this paper we formulate the problem of testability characterization in reconvergence-free NAND gate circuits consisting of gates with arbitrary fanins. Analytical relationships between aggregate measures of structural characteristics of a circuit and its controllability properties is established. The distribution of controllability of gates in different circuit levels is characterized. Limiting values of expected controllabilities and rates of convergence to these values under different conditions are obtained. In doing so, a statistical model for fanins of gates in a circuit is formulated and verified. Conditions under which these results are applicable to general NAND circuits (with reconvergent fanouts) are also presented. It is shown that the accuracy of these predictions, as approximations to controllability in general NAND circuits, improves as the distance between fanout stems and the point of their reconvergence increases. Extensions of these results to other reconvergence-free homogeneous (AND, OR and NOR gate) circuits are also presented.

The distribution of primary input fault observability is characterized and the problems of determining the optimal weight of random input patterns that maximize the expected observabilities and expected primary input fault coverage, are also addressed.
1 Introduction

Testing of circuits using a sequence of random input patterns has emerged as a popular test methodology. The effectiveness of this method of testing is indicated by the number of faults that are tested for (termed fault coverage) by a sequence of random patterns. In order to estimate fault coverage of a circuit under test, prior testability analysis of the circuit is carried out. Testability analysis consists of two independent tasks; 1) controllability computation (probability of activating a fault) and 2) observability computation (probability of propagating a fault to a primary output).

Testability analysis techniques found in the literature [3,5,7,6,8] propose algorithms to compute estimates of controllabilities and observabilities of individual lines. Circuits are viewed as a set of completely heterogeneous gates and a procedural relation (or procedural characterization), between testability of gates and circuit structure, is established. The main drawback of these procedures is that, in order to determine the effects, of changing the circuit, on its testability, one needs to run a procedure.

We address the fundamental problem of establishing an analytical relation between testability of a circuit and its structure. The importance of such a characterization lies in the fact that, in order to determine the effects of changes in circuit structure on testability, one needs to evaluate a function. Such a process is expected to require much less time than evaluating a procedural relation.

In this paper we focus on establishing a analytical relationship between testability in circuits with the same type of gates (homogeneous circuits), and some statistical characteristics of circuit structure. In particular we consider reconvergence-free NAND circuits and characterize a relationship between the controllability of a gate in level $i$ of the circuit and the distribution of fanins of gates in that circuit. We also discuss conditions under which this characterization is applicable to NAND circuits with reconvergent fanouts. Next, we use these controllability properties to characterize a relationship among circuit structure, observability and fault coverage.

Our choice of NAND gate circuits is influenced by the fact that most gate array structures use NAND gates. Moreover, PLA's and several other circuit structures can be modelled easily as NAND circuits. The results of this paper are especially applicable to
circuits undergoing built-in random or pseudo-random self test. We also provide extensions of our results to other homogeneous (AND, OR and NOR) circuits.

Characterization of testability properties using controllability behaviour of gates was first studied in [1]. The authors considered regular NAND trees consisting of gates with the same number of inputs. The behaviour of controllability of gates in different levels is used to compute the probability of detecting faults in primary input lines.

Recently, in [4], the authors consider a tree consisting of alternate levels of \( m \)-input AND gates and \( n \)-input OR gates. Such a circuit is quite similar to the ones considered in [1], differing in the fact that gates in alternate levels in the circuit have different number of inputs. This is because a level of AND gates followed by a level of OR gates can be converted to two consecutive levels of NAND gates without changing the function, by including two inverters on the output of each AND gate.

Thus the class of circuits considered in [1] can be derived as special cases of those considered in [4] by setting \( m = n \). In [4], the authors define a controllability transfer function (SPTF) which expresses the controllability of a gate in terms of the controllabilities of gates in the previous level. This function is used to obtain limits of controllabilities of gates as the number of levels in the circuit increases.

In this paper we present a complete generalization of the results presented in [1,4]. Our generalization is obtained by considering circuits consisting of gates with arbitrary fanins. We characterize the distribution of controllabilities of gates in different levels of reconvergence-free NAND gate circuits. Criteria under which these results can be used for general NAND circuits (with reconvergent fanouts) are also discussed. Functions similar to the SPTF (see [4]) are defined and used to find limits of the expected controllabilities of gates as the number of levels increases. We also present some results on determining primary input controllabilities in order to maximize primary input observabilities and expected fault coverage. We assume that all the primary outputs have the same distance \( L \) (in levels of gates) from the primary inputs.

The paper is organized as follows. Section 3 provides an analysis for controllability behaviour in a reconvergence-free NAND gate circuit. In doing so we also formulate, in Section 4, a statistical model for the structure of a circuit and provide results on the
limiting behaviour of expected controllabilities. Results on speed of convergence to limiting controllability values are given in Section 4.2. In Section 6, we discuss conditions under which these results are applicable to general NAND circuits which may have reconvergent fanouts. Next, in Section 7, we state, without proof, some results extending the above model to other reconvergence-free homogeneous circuits. In Section 8, we present simulation results and compare them with theoretical predictions of our model. In Section 9, we present results on characterizing observability of faults in terms of circuit parameters. The problems of determining the weight of random patterns that maximize observability and expected fault coverage in such circuits are also addressed in this section. We present some concluding remarks in Section 10.

In order to smoothen the flow of the text, we have included most of the lengthy proofs of results in the appendices.

2 Notation

*Definition:* 1-controllability (or signal probability) of a line in a circuit is the probability that the line has a logic value ‘1’ at any time.

*Definition:* 0-controllability (or 0-signal probability) of a line in a circuit is the probability that the line has a logic value ‘0’ at any time.

*Definition:* Fault Coverage $F_S$ of a set $S$ of faults is $\frac{|S'|}{S}$ when $S'$ is the subset of faults that have been tested for.

\[
\begin{align*}
E[.] & \quad \text{Expected value of a random variable.} \\
Var(.) & \quad \text{Variance of a random variable.} \\
pgf & \quad \text{Probability generating function} \\
mgf & \quad \text{Moment generating function.} \\
X & \quad \text{Random variable representing the fanin of a gate in the circuit.} \\
g_X(s) & \quad \text{Probability generating function of } X. \\
g_X^{(n)}(s) & \quad \underbrace{g_X(g_X \cdots (g_X(s)) \cdots).}_{n \text{ times}} 
\end{align*}
\]
$$h(s) = 1 - g_X(s).$$

$$f(s) = h(h(s)) = 1 - g_X (1 - g_X(s)).$$

$$r(s) = \frac{g_X(s)}{s}.$$

$$Y_i$$ Random variable representing the 1-controllability of a line in level $i$ of a reconvergence-free NAND gate circuit.

$$\mu_i^{(m)}$$ $m$th moment of the random variable $Y_i$.

$$\mu_i^{(1)}$$ the 1st moment of $Y_i$.

$$d$$ The distance, in number of gate levels, between a stem and a line in its fanout path.

$$Z_i$$ Random variable representing the 1-controllability of a line in level $i$ of a reconvergence-free AND circuit.

$$\eta_i^{(m)}$$ $m$th moment of the random variable $Z_i$.

$$\hat{Y}_i$$ Random variable representing the 0-controllability of a line in level $i$ of a reconvergence-free NOR circuit.

$$\hat{Z}_i$$ Random variable representing the 0-controllability of a line in level $i$ of a reconvergence-free OR circuit.

$$W_i$$ Random variable representing the probability of a fault-effect propagating through a gate in level $i$.

$$V$$ Random variable representing observability of a fault on a primary input line.

$$I$$ The set of primary input lines $|I| = N_I$.

$$F_I$$ Random variable representing primary input fault coverage.

$$\xi_{j,v,\tau}$$ Indicator random variable for detection of $s\cdot a\cdot v$ fault on primary input line $j$ in $\tau$ test clock cycles.

## 3 Controllability of General Reconvergence-Free NAND Gate Circuits

In this section we present an analysis for characterization of controllability in NAND gate circuits without reconvergent fanout or feed-forward. The reconvergence-free condition restricts our analysis to the case when the values at the inputs of a gate are statistically independent. The assumption of zero feed-forward does not impose any restrictions on circuits since a circuit with feed-forward can be converted to one without any, by simply adding buffers in the feed-forward lines. Therefore, the class of circuits we consider consists of all NAND gate circuits with gates having arbitrary fanins and no reconvergent fanouts. In this respect the following analysis provides a complete generalization of the results presented in [1,4].
The controllability at the output of a gate is a function of the controllabilities at its inputs. For a NAND gate the output controllability $Y$ is one minus the product of the input controllabilities and therefore it also depends on the number of inputs. In our analysis we assume that the number of inputs to a gate in the circuit is a random quantity and is represented by the random variable $X$. Since $Y$ is a function of $X$, $Y$ is also a random variable.

Given that the controllabilities at the primary inputs are independent and identically distributed (iid), the structure of a reconvergence-free NAND circuit, implies that the random variables $Y_A$ and $Y_B$, associated with two gates $A$ and $B$ at the same level, are iid. We now proceed to develop a rigorous characterization for controllabilities of gates in a level $i$ of the circuit. This characterization is based on the distribution of fanins of gates and the distribution of primary input controllabilities.

Let $Y_i$ be a continuous random variable in $[0,1]$ representing the controllability of a gate in level $i$. Let the number of inputs to the gate be $k$, i.e. $k$ is a realization of the random variable $X$ defined above. Since there is no feed-forward in the circuit, the level at which these inputs are located is $i - 1$. Let $Y_{i-1,j}$ represent the controllability at input $j$ ($j = 1 \ldots k$) of the gate. We can express $Y_i$ as

$$Y_i|_{X=k} = 1 - Y_{i-1,1}Y_{i-1,2}\cdots Y_{i-1,k}.$$  \hspace{1cm} (1)

The following theorem expresses the moments of $Y_i$ in terms of the pgf of $X$.

**Theorem 1:** Let the $m$th moment of $Y_i$ be denoted by $\mu_i^{(m)}$, i.e. $\mu_i^{(m)} = E[(Y_i)^m]$. Then

$$\mu_i^{(m)} = \sum_{j=0}^{m} (-1)^j \binom{m}{j} g_X(\mu_{i-1}^{(j)})$$  \hspace{1cm} (2)

where $g_X(s)$ is the probability generating function (pgf) of the random variable $X$, i.e.

$$g_X(s) = \sum_{k=1}^{\infty} s^k P\{X = k\} = \sum_{k=1}^{\infty} s^k p_k.$$  

**Proof:** (see Appendix A)

Equation (2) expresses the $m$th moment of $Y_i$ in terms of $j$th moment ($j = 0 \ldots m$) of $Y_{i-1}$ and the characterizing function is $g_X(s)$, the pgf of $X$. Let the function
\[ h(s) = 1 - g_X(s). \] From Equation (2) we can express the expected value \( E[Y_i] \) of the controllability \( Y_i \) at level \( i \) as

\[ E[Y_i] = \mu_i^{(1)} = 1 - g_X(\mu_{i-1}^{(1)}) = h(\mu_{i-1}^{(1)}) \quad (3) \]

and its variance as

\[
Var(Y_i) = \mu_i^{(2)} - \left(\mu_i^{(1)}\right)^2
\]

\[
= 1 - 2g_X(\mu_{i-1}^{(1)}) + g_X(\mu_{i-1}^{(2)}) - \left(1 - g_X(\mu_{i-1}^{(1)})\right)^2
\]

\[
= g_X(\mu_{i-1}^{(2)}) - \left(g_X(\mu_{i-1}^{(1)})\right)^2. \quad (4)
\]

We now examine the behaviour of the expected controllability at different levels of the circuit. We show that under certain conditions the distribution of controllability degenerates to the mean value as the levels of logic increase. From Equations (2) and (3), we see that \( \mu_i^{(1)} \) is determined from the pgf \( g_X(s) \) of fanins. We now show that behaviour of the expected controllability is determined by the fixed points of \( 1 - g_X(s) \). In the rest of the paper we use the symbols \( \mu_i \) and \( \mu_i^{(1)} \) interchangeably.

3.1 Behaviour of Expected Controllability

The initial results that we present here make no assumptions on the distribution of \( X \) and therefore the sample space of circuits that these results are applicable to, are all NAND circuits with no reconvergent fanouts. As we proceed with our analysis we shall need to impose some constraints on the distribution of \( X \) in order to obtain further results. The effect of this is that the space of circuits to which these results apply is restricted. Nevertheless, it is shown that most circuits satisfy these additional restrictions and thus in spite of these constraints the sample space considered is, for all practical purposes, quite rich.

Let \( g_X(s) \) be the pgf of \( X \) and \( h(s) = 1 - g_X(s) \). Also, let \( f(s) = h(h(s)) \) and \( f^{(k)}(s) \) denote the \( k \)th composition of \( f(s) \). We first state some properties of the functions \( g_X(s) \), \( h(s) \) and \( f(s) \), that will be useful in obtaining results concerning \( \mu_i \).

**Lemma 1:**
a) \( g_X(s) \) is monotonically increasing for \( s \in [0,1] \) and is strictly increasing when \( p_1 = P\{X = 1\} > 0 \).

b) \( g_X(s) \) is convex for \( s \in [0,1] \).

c) \( g_X(s) \) has exactly two fixed points, namely \( s = 0 \) and \( 1 \) in the interval \( [0,1] \).

d) \( h(s) \) has exactly one fixed point \( p \) for \( s \in (0,1) \).

Proof: (see Appendix A) 

\[ \square \]

**Theorem 2:**

a) \( q \) is a fixed point of \( f(s) \) if and only if \( h(q) \) is also a fixed point of \( f(s) \).

b) \( f(s) \) has at least one fixed point in the open interval \( (0,1) \) and therefore at least three fixed points in the closed interval \( [0,1] \).

c) \( \left( f^{(k)}(s) \right) \) is monotonically increasing and

\[ \left( f^{(k)}(s) \right)'(0) = \left( f^{(k)}(s) \right)'(1) = \left[ \frac{g'_{\lambda}(1)}{g'_{\lambda}(0)} \right]^k. \]  \hspace{1cm} (5)

Proof: (see Appendix A) 

\[ \square \]

We can now prove the following characteristics of the behaviour of \( \mu_i \).

**Theorem 3:** Let \( p \) be the unique fixed point of \( h(s) \) (see Lemma 1d).

a) If \( \mu_{i-1} < p \) then \( \mu_i > p \) and vice versa.

b) Further, if \( \mu_j = p \) for some \( j \geq 0 \) then \( \mu_i = p \) \( \forall i \geq j \).

**Proof:** Proof of a) is as follows. From Equation (3) \( \mu_i = h(\mu_{i-1}) \). Since \( h(s) = 1 - g_X(s) \) and \( g_X(s) \) is monotonically increasing (by Lemma 1a), we can see that \( h(s) \) is monotonically decreasing. Let \( \mu_{i-1} < p \). Then \( \mu_i = h(\mu_{i-1}) > h(p) = p \). Similarly, if \( \mu_{i-1} > p \) then \( \mu_i = h(\mu_{i-1}) < h(p) = p \). Part b) is obvious since \( p \) is the fixed point of \( h(s) \).  \[ \square \]

From this theorem we can conclude that if \( \mu_0 < p \) then \( \mu_1 > p \) and \( \mu_2 < p \) and so on. In this case the expected controllabilities of all even numbered levels will be less than \( p \) and those of all odd numbered levels greater than \( p \). Similarly if \( \mu_0 > p \) then the expected controllabilities of all even numbered levels will be greater than \( p \) and those of all odd numbered levels less than \( p \).
We can conclude the following from Theorem 3. If \( \mu_0 = p \), then the expected controllabilities of all levels remain the same. However, if \( \mu_0 \neq p \), then the set of gates can be dichotomized into gates at even numbered levels and those at odd numbered levels. Therefore, Theorem 3 provides a partial description of the expected controllabilities when \( \mu_0 \neq p \). To obtain a complete description, for this case, the behaviour of expected controllabilities in each of the two sets must be examined.

We now establish a relation between \( \mu_i \) and \( \mu_{i-2} \). From Equation (3) we can express \( \mu_i \) as

\[
\mu_i = 1 - g_x(\mu_{i-1}) = 1 - g_x(1 - g_x(\mu_{i-2})) = f(\mu_{i-2})
\]  

(6)

From Theorem 2, it is straightforward to establish the following properties:

1. If \( p \in (0,1) \) is the fixed point of \( h(s) \) (and therefore also of \( f(s) \)). Then,

\[
\mu_k = p \Rightarrow \mu_{k+i} = p \quad \forall \; i \geq 0.
\]

2. Suppose \( f(s) \) has \( j \) (\( > 1 \)) fixed points in the open interval \( (0,1) \). Let \( q \in (0,1) \) (\( q \neq p \)) be one of the \( j \) fixed points. If the expected controllability at some level \( k \) equals \( q \), then the expected controllability at level \( k + 2i \) (\( i \geq 0 \)) equals \( q \). Furthermore, by Theorem 2a, the expected controllability at levels \( k + (2i + 1) \) equals \( h(q)(\neq p)(\neq q) \), where \( h(q) \) is one of the fixed points of \( f(s) \).

We now consider the controllability characteristics of circuits in which fanins of gates follow a distribution restricted to a parametric family. The parametric family that we consider is that of generalized geometric distribution.

### 4 Controllabilities for a Particular Distribution of Fanins

The analysis upto now did not assume any particular distribution of gate fanins. Examination of a large number of benchmark circuits [2] (see Section 8.1) indicates that a generalized geometric distribution provides an excellent model for describing the random variable \( X \). It was found that the proportion of 1-input gates (buffers and inverters) in different circuits can vary over a large range. However, the number of \( n \)-input gates (\( n > 1 \)) follows an approximate geometric law. In this section we examine the behaviour of controllabilities when the fanins follow such a distribution.
Figure 1: Different shapes of the generalized geometric distribution for different values of parameters.

The probability mass function (pmf) of a generalized geometric random variable is given by

\[ P_k = \begin{cases} \frac{a}{(1-a)(1-b)} & \text{if } k = 1 \\ b^{k-2} & \text{if } k > 1. \end{cases} \]  \hspace{1cm} (7)

The standard (pure) geometric distribution is obtained when \( b = 1 - a \) in Equation (7). The functions \( p_k \) for different values of \( a \) and \( b \) are shown in Figure 1. The pgf of \( X \), denoted by \( g_X(s) \) and the functions \( h(s) \) and \( f(s) \) are given by

\[ g_X(s) = a s + \frac{(1-a)(1-b)s^2}{1-bs} \] \hspace{1cm} (8)

\[ h(s) = \frac{(1-s)(1+(1-a-b)s)}{1-bs}. \] \hspace{1cm} (9)

\[ f(s) = \frac{P(s)Q(s)}{R(s)}. \] \hspace{1cm} (10)

where

\[ P(s) = [(1-bs) - (1-s)(1+(1-a-b)s)] \]

\[ Q(s) = [(1-bs) + (1-a-b)(1-s)(1+(1-a-b)s)] \]

\[ R(s) = (1-bs)^2 - b(1-s)(1-bs)(1+(1-a-b)s). \]
The expected value of $X$ is

$$E[X] = \left. \frac{d}{ds} g_X(s) \right|_{s=1} = 1 + \frac{1 - a}{1 - b}. \tag{11}$$

In Section 8.1 we provide empirical evidence for the use of the generalized geometric distribution. The parameters $a$ and $b$ in Equation (7) are easily estimated from fanin data of gates in a circuit using the method of *maximum likelihood* and is discussed in Appendix F.

We now proceed with the analysis of the function $f(s)$ that will yield further insight into the behaviour of the expected controllabilities of gates within each of the two partitions (i.e. gates in even and odd numbered levels) mentioned previously.

From Equation (10), it is easy to show that when $X$ follows a *pure geometric distribution* (i.e. $a + b = 1$) then the function $f(s)$ reduces to $f(s) = s$. In this case every point $s \in [0,1]$ is a fixed point of $f(s)$. Thus, if $a + b = 1$, a complete characterization of expected controllabilities is as follows.

$$\mu_{2i} = \mu_0 \quad \& \quad \mu_{2i+1} = \mu_1 = h(\mu_0) \quad i = 1, 2, \ldots$$

When $a + b \neq 1$, we need to study the characteristics of the function $f(s)$. From Theorem 2b, we know that $f(s)$ has at least three fixed points in the interval $[0, 1]$. When $X$ follows a *generalized geometric distribution*, all the possible functions $f(s)$ can be partitioned into exactly two classes, depending on the number of fixed points it has. This is stated in Lemma 2.

**Lemma 2:** Let $X$ follow a generalized geometric distribution with parameters $a$ and $b$. Then

a) if $a + b = 1$, $f(s) = s$ and every point $s \in [0,1]$ is a fixed point of $f(s)$, and

b) if $a + b \neq 1$, $f(s)$ has exactly three fixed points in $[0, 1]$, namely $s = 0, 1$ and $p$ where $p$ is the unique fixed point of $h(s)$.

**Proof:** (see Appendix B) \(\square\)

Lemma 2 allows us to give a complete characterization of expected controllabilities $\mu_i$, if the expected controllability $\mu_0$ (at the primary inputs) equals one of the fixed points of
$f(s)$. Our interest is in determining the behaviour of $\mu_i$ when $\mu_0$ is not one of these points. This is discussed in the following section. It also leads to a characterization of the limiting behaviour of expected controllabilities as the number of levels (of NAND gates) increases.

### 4.1 Limiting Behaviour of Controllabilities

In the following analysis we assume that $X$ follows a generalized geometric distribution whose pmf is given by Equation (7).

In Lemma 2, it was shown that the set of functions $f(s)$ can be partitioned into two subsets, by the number of fixed points it has. In the following theorem, we show that the set of functions $f(s)$, can be partitioned into three subsets according to the value of $(a + b)$. Before stating the theorem, we first relate $f'(0)$ to the value of $(a + b)$ in the following lemma.

**Lemma 3:** Let $a < 1$. Then $f'(0) < 1(= 1)[> 1]$ if and only if $a + b < 1(= 1)[> 1]$.

**Proof:** (see Appendix B) \[ \square \]

**Theorem 4:** Let $f'(0) \neq 1$. Further, let $p$ be the fixed point of $h(s)$ in the open interval $(0,1)$. Define $I_1 = (0, p)$ and $I_2 = (p, 1)$. Then $f(s) < s$ for $s \in I_1$ and $f(s) > s$ for $s \in I_2$ if and only if $f'(0) < 1$. Furthermore, $f(s) > s$ for $s \in I_1$ and $f(s) < s$ for $s \in I_2$ if and only if $f'(0) > 1$.

**Proof:** We present the proof only for the case when $f'(0) < 1$. The proof for the other case is similar.

The proof of the necessary condition is as follows. We know that $f(0) = 0$. Thus, given that $f(s) < s$ for $s \in I_1$ and that $f(s)$ is continuous, by definition, for some $\epsilon \in (0, p)$ we have

\[
 f'(0) = \lim_{\epsilon \to 0} \frac{f(\epsilon) - f(0)}{\epsilon - 0} \\
 = \lim_{\epsilon \to 0} \frac{f(\epsilon)}{\epsilon} \\
 < \lim_{\epsilon \to 0} \frac{\epsilon}{\epsilon} = 1.
\]

The proof of the sufficient condition is as follows. Using Lemma 7 (see Appendix C) it
is enough to show that, given $f'(0) < 1$, we can find points $\zeta_1 \in I_1$ and $\zeta_2 \in I_2$ such that $f(\zeta_1) < \zeta_1$ and $f(\zeta_2) > \zeta_2$. Suppose there is no point $\zeta_1 \in I_1$ such that $f(\zeta_1) < \zeta_1$. This implies that $f(s) > s$ for all $s \in I_1$. In that case, since $f(s)$ is continuous, by definition of first derivative, we have for some $\epsilon \in (0, p)$

$$f'(0) = \lim_{\epsilon \to 0} \frac{f(\epsilon) - f(0)}{\epsilon - 0}$$

$$= \lim_{\epsilon \to 0} \frac{f(\epsilon)}{\epsilon}$$

$$> \lim_{\epsilon \to 0} \frac{\epsilon}{\epsilon} = 1.$$  

This is a contradiction.

Similarly assume there is no point $\zeta_2 \in I_2$ such that $f(\zeta_2) > \zeta_2$. This implies that $f(s) < s$ for all $s \in I_2$. We are given that $f(1) = 1$. In that case, since $f(s)$ is continuous, we can express $f'(1)$ for some $\epsilon < 1 - p$ as

$$f'(1) = \lim_{\epsilon \to 0} \frac{f(1) - f(1 - \epsilon)}{1 - (1 - \epsilon)}$$

$$= \lim_{\epsilon \to 0} \frac{1 - f(1 - \epsilon)}{\epsilon}$$

$$> \lim_{\epsilon \to 0} \frac{1 - (1 - \epsilon)}{\epsilon} = 1.$$ 

But by Theorem 2c, we know that $f'(1) = f'(0) < 1$. This is a contradiction. Therefore if $f'(0) < 1$ then $f(s) < s$ for all $s \in I_1$ and $f(s) > s$ for all $s \in I_2$. This proves the theorem.

**Corollary:** (to Theorem 4) Let $p$ be the fixed point of $h(s)$ in the open interval $(0,1)$. Define $I_1 = (0, p)$ and $I_2 = (p, 1)$. Then

a) $f(s) < s(> s)$ for $s \in I_1(I_2)$ if and only if $a + b < 1$.  

b) $f(s) = s$ for $s \in [0, 1]$ if and only if $a + b = 1$.

C) $f(s) > s(< s)$ for $s \in I_1(I_2)$ if and only if $a + b > 1$.

**Proof:** This follows directly from Lemma 3 and Theorem 4.
Figure 2: S-shaped curve for \( f(s) \) when \( f'(0) < 1 \).

When \( a + b = 1 \), we had presented, earlier, a complete characterization of expected controllabilities in different levels of a reconvergence-free circuit. We can now present the characteristics of expected controllabilities when \( a + b \neq 1 \). Before discussing the impact of the above results on the limiting behaviour of controllability we briefly recapitulate our findings and some of the relevant implications about the function \( f(s) \) when \( a + b \neq 1 \).

Using Lemma 2 and Theorem 4, we have for \( s \in [0,1] \):

1) \( f(s) \) is monotonically increasing.
2) If \( a + b \neq 1 \) then \( f(s) \) has exactly three fixed points.
3) If \( a + b < 1 \) then \( f(s) < s \) for \( s \in I_1 \) and \( f(s) > s \) for \( s \in I_2 \).
4) If \( a + b > 1 \) then \( f(s) > s \) for \( s \in I_1 \) and \( f(s) < s \) for \( s \in I_2 \).

Properties 3) and 4) above suggest that if \( a + b < 1 \) then \( f(s) \) is an S-shaped curve and if \( a + b > 1 \) then \( f(s) \) is a curve whose reflection along the \( y = s \) line is S-shaped (see Figures 2 and 3).

As an example let us consider a reconvergence-free NAND circuit where gates have fanins distributed according to a generalized geometric distribution with parameters \( a = 0.1 \) and \( b = 0.3 \). The shape of the function \( f(s) \) is shown in Figure 2. Similarly for a circuit with parameters \( a = 0.7 \) and \( b = 0.8 \) the shape of the curve \( f(s) \) is shown in Figure 3.

The following theorem provides the main result about the limiting behaviour of \( \mu_i \).

**Theorem 5:** Let \( p \) be the fixed point of \( h(s) \) in the interval \((0,1)\) and let \( a + b \neq 1 \). Then

\textbf{a}) If } \( \mu_0 = p \) \textbf{ then } \( \mu_i = p \ \forall \ i \geq 0 \).
b) If $a + b > 1$ and $\mu_0 \neq 0,1$ or $p$, then $\lim_{i \to \infty} \mu_i = p$.

c) If $a + b < 1$ and $\mu_0 \neq 0,1,p$ then given that $\mu_0 < p(>p)$, $\lim_{i \to \infty} \mu_{2i} = 0(1)$ and $\lim_{i \to \infty} \mu_{2i+1} = 1(0) \forall i \geq 0$.

Proof: (see Appendix B)

We have presented a characterization of the behaviour of the expected value of controllabilities at different levels of a NAND gate circuit. In summary, we see that, if the fanins $X$, of gates in a reconvergence-free NAND circuit follow a generalized geometric distribution with parameters $a$ and $b$, then the following behaviour of expected controllabilities can be observed.

1) If $a + b < 1$, the expected controllabilities at alternate levels of the circuit progressively converge to 0 and 1 respectively. This means that if two consecutive levels are chosen "far enough" from primary inputs then the expected controllabilities at these two levels are either respectively 0 and 1 or 1 and 0. This phenomenon is a generalization of the one shown in [1,4].

2) If $a + b = 1$, the expected controllabilities in alternate levels remain the same. This is the case when the distribution of $X$ is the unmodified geometric distribution.

3) If $a + b > 1$, the expected controllabilities at different levels progressively converge to a value $p$ ($0 < p < 1$) determined by $a$ and $b$. This occurs when either the number of inverters in a NAND circuit is large or when the disparity among the proportions of gates with different fanins is small.

Cases 2 and 3 above are novel results in the area of controllability characterization in reconvergence-free NAND gate circuits. Apart from relating structure to controllabilities in different levels of a circuit, it also adds to the current knowledge of controllability behaviour.
Furthermore, as shown in Section 5, the framework assumed in [1,4] can be considered as special cases of Case 1 above.

When \( a + b < 1 \) (Case 1), the expected controllability of gates "far" from the primary inputs is close to 1 or 0. This also implies that the distribution of controllability for gates degenerates as the level at which they are located increases. This is proved in the following theorem.

**Theorem 6:** Let parameters \( a \) and \( b \) be such that \( a + b < 1 \). Then \( \lim_{i \to \infty} \text{Var}(Y_i) = 0 \).

**Proof:** (see Appendix B)

Theorem 6 allows us to conclude that a gate sufficiently far from the primary inputs is expected to have a controllability of either 1 or 0. This means that such a gate will have either a logic 1 or a logic 0 at all times regardless of the input pattern applied. Such limiting behaviour of controllabilities has a great impact on the testability of the circuit and is discussed in Section 9.

### 4.2 Rate of Convergence of Expected Controllabilities

In Section 4.1, we presented an analysis for the limiting behaviour of expected controllabilities. It was found that, if fanins of gates follow a generalized geometric distribution then the expected controllabilities of gates in different levels in the circuit converge to one or more of the fixed points of \( f(s) \), as the number of levels in the circuit increases.

In this section we focus on estimating the level \( N \) of the circuit at which the expected controllability \( \mu_N \) of gates is "close enough" to its limiting value, i.e. if \( l \) is a limiting value of expected controllabilities then we want to estimate \( N \) such that \( |\mu_N - l| < \epsilon \) for a given \( \epsilon > 0 \). The cases of interest are when the parameters \( a \) and \( b \) of the fanin distribution are such that \( a + b \neq 1 \) and \( \mu_0 \) is different from any of the fixed points of the function \( f(s) \). We consider only the case when \( a + b < 1 \), since the technique for estimating \( N \) for \( a + b > 1 \) is similar.

When \( a + b < 1 \), then by Lemma 2, \( f(s) \) has exactly three fixed points, namely 0,1 and \( p \), where \( 0 < p < 1 \). If \( \mu_0 < p \) then, as shown in Section 4.1, \( \mu_{2i} \)'s (\( i = 0, 1, \ldots \)) converge to 0 and \( \mu_{2i+1} \)'s converge to 1 as \( i \to \infty \). Thus, given an \( \epsilon \), we want to estimate \( N0(\epsilon) \) and
Figure 4: Piecewise linear approximation of \( f(s) \).

\( N1(\epsilon) \) such that for \( i > N0(\epsilon) \), \( \mu_{2i} < \epsilon \) and for \( j > N1(\epsilon) \), \( 1 - \mu_{2j+1} < \epsilon \). We now show the estimation of \( N0(\epsilon) \). Estimation of \( N1(\epsilon) \) can be done in a similar manner. Further, estimation of \( N0(\epsilon) \) and \( N1(\epsilon) \) when \( \mu_0 > p \) will also be clear from the following discussion.

Let \( a + b < 1 \) and \( \mu_0 < p \). Then, as shown in Section 4, \( \mu_2 = f(\mu_0) < \mu_0 \), \( \mu_4 = f^{(2)}(\mu_0) < \mu_2 \) and in general \( \mu_{2i} = f^{(i)}(\mu_0) < \mu_{2i-2} \), where superscript \( (i) \) of function \( f \) indicates the \( i \)th composition of that function. Thus, given \( \epsilon \), \( N0(\epsilon) \) is the least number such that \( f^{(N0(\epsilon))}(\mu_0) < \epsilon \).

Let \( p \) be the fixed point of \( f(s) \) in the interval \((0, 1)\) and let \( z = \frac{p f'(p) - 1}{f'(p) - f'(0)} \). We define \( P(s) \) as

\[
P(s) = \begin{cases} 
A(s) = f'(0)s & s \in [0, z) \\
B(s) = f'(p)s + p(1 - f'(p)) & s \in [z, p]
\end{cases}
\]

\( P(s) \) is illustrated in Figure 4 for some \( f(s) \). We can now prove the following.
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Table 1: Estimates of \( NO(\epsilon) \) for different \( \epsilon \) and \( \mu_0 \) and two different parameter values.

Lemma 4:

\[
NO(\epsilon) \approx \overline{NO}(\epsilon) = \begin{cases} 
\left[ \log \left( \frac{\epsilon}{\mu_0} \right) / \log(f'(0)) \right] & \mu_0 < z \\
\log \left( \frac{\epsilon f(0) - \frac{r^p - r}{m}}{\mu_0 - \frac{r^p - r}{m}} \right) + \frac{\log(\frac{\epsilon}{\mu_0})}{\log(f'(0))} & \mu_0 \geq z 
\end{cases}
\]

where \( m = f'(p) \) and \( c = p(1 - f'(p)) \).

Proof: (see Appendix B) \( \square \)

Table 1 shows values of \( \overline{NO}(\epsilon) \) for different values of \( \epsilon \) and \( \mu_0 \). We can see that these estimates of \( NO(\epsilon) \) are quite accurate. However, it is clear that the accuracy of these predictions will depend on the slope \( f'(0) \) and also on the starting point \( \mu_0 \).

The main effect, of the limiting values of controllabilities in a circuit, is on its testability. Since \( NO(\epsilon) \) is the level of circuit, beyond which the expected controllability falls below \( \epsilon \), it also indicates the level beyond which the respective probabilities of 1) propagation of faults through gates in the next level and 2) activating \( s-a-0 \) faults on lines in that level, falls below a certain quantity depending on \( \epsilon \) and the distribution of \( X \). On the other hand, \( N1(\epsilon) \) indicates the circuit level beyond which the probability of activating \( s-a-1 \) faults falls below a certain quantity. Thus both \( NO(\epsilon) \) and \( N1(\epsilon) \) can be used as measures of testability of the circuit.

We now prove the following relation between \( NO(\epsilon) \) and \( N1(\epsilon) \).

Proposition 1: Let parameters \( a \) and \( b \) be such that \( a + b < 1 \). Given \( \epsilon > 0 \),
\[ N0(\epsilon) \geq N1(\epsilon). \]

**Proof:** Assume \( \mu_0 < p \) (the proof for the case when \( \mu_0 > p \) is similar). Therefore, by Theorem 5, \( \mu_{2i} \)'s approach 0 and \( \mu_{2i+1} \)'s approach 1. By definition \( \mu_{2i} > (\leq) \epsilon \) for \( i < (\geq) N0(\epsilon) \). Similarly \( \mu_{2i+1} < (\geq) 1 - \epsilon \) for \( i < (\geq) N1(\epsilon) \). Suppose \( N0(\epsilon) < N1(\epsilon) \). This implies that
\[
\mu_{N0(\epsilon)+1} = h(\mu_{N0(\epsilon)}) < 1 - \epsilon.
\]

But by definition \( \mu_{N0(\epsilon)} \leq \epsilon \). Since by Lemma 1, \( h(s) \) is a monotonically decreasing function,
\[
h(\mu_{N0(\epsilon)}) > h(\epsilon) = 1 - g_X(\epsilon).
\]

We know that \( g_X(s) < s \) for \( s \in (0,1) \). Thus from the above inequation, we can see that
\[
\mu_{N0(\epsilon)+1} = h(\mu_{N0(\epsilon)}) > 1 - \epsilon.
\]

This is a contradiction. Therefore, \( N0(\epsilon) \geq N1(\epsilon) \).

Thus, we see that if we are considering only fault propagation characteristics as a measure of testability of the circuit, we need to estimate \( N0 \). However if we are interested also in the probability of fault activation, then we need to estimate \( N1 \) since by the above proposition \( N1 \leq N0 \).

We now present an analysis of earlier work done in the area of controllability characterization as special cases within the above general framework.

## 5 Analysis of Circuits in [1] and [4] as Special Cases

Consider a logic tree consisting of NAND gates each with \( n \) inputs (as studied in [1]). In this case the distribution of \( X \) can be expressed as
\[
P\{X = k\} = \begin{cases} 0 & k \neq n \\ 1 & k = n \end{cases}.
\]

We can thus see that
\[
g_X(s) = \sum_{k=1}^{\infty} p_k s^k = s^n \tag{14}
\]
\[
h(s) = 1 - s^n \tag{15}
\]
\[
f(s) = 1 - (1 - s^n)^n.
\]

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Let the primary input controllability be deterministic. This means that the controllabilities at all levels are deterministic and therefore \( Y_i = \mu_i \). For \( n > 1 \), we can see from Theorem 2c that \( f'(0) = f'(1) = 0 < 1 \). Let us assume \( \mu_0 \neq p \) where \( p \) is the fixed point of the function \( h(s) \) as expressed in Equation (15). Then, according to Theorem 5c) the limiting value of \( \mu_i \) is 0 and 1 respectively for alternate levels \( i \) and \( i + 1 \). If \( \mu_0 = p \) then \( \mu_i \) is identically equal to \( p \) for all \( i \). For each \( n \) we can obtain \( p \) by solving for \( s \) in the equation

\[
h(s) - s = 1 - s^n - s = 0.
\]

Thus for \( n = 2 \) we get \( p = 0.618 \) as found in [4].

Let us now consider regular AND-OR trees studied in [4]. As mentioned in Section 1, such trees are the same as NAND trees. In [4], the trees considered, have alternate levels of \( n \)-input AND gates and \( m \)-input OR gates. This translates to a NAND tree consisting of alternate levels of \( n \)-input gates and \( m \)-input gates. An implicit assumption is that if level-0 consists of OR gates, we consider the circuit from level-1 onwards.

For the levels consisting of \( n \) \((m)\)-input NAND gates the pmf of \( X \) can be expressed as

\[
P\{X = k\} = \begin{cases} 0 & k \neq n \ (m) \\ 1 & k = n \ (m) \end{cases}.
\]  

Thus we have two different pgf's for the two distributions. Labelling the two random variables as \( X_m \) and \( X_n \) we have

\[
g_{X\theta} = s^\theta \tag{17}
\]

\[
h_{\theta}(s) = 1 - s^\theta \tag{18}
\]

where \( \theta = m, n \). Thus the results of [4] can now be obtained by assuming the degenerate pmf for fanins given by Equation (16).

The function \( f(s) \) relating \( \mu_i \) to \( \mu_{i-2} \) can be expressed in two ways. Distinguishing between the two forms by labelling them \( f_m(s) \) and \( f_n(s) \) we can express these as

\[
f_m(s) = 1 - (1 - s^m)^n = h_n(h_m(s))
\]

\[
f_n(s) = 1 - (1 - s^n)^m = h_m(h_n(s)).
\]
These functions are identical to the transfer functions considered in [4]. It is easy to show that \( f_m'(0) = f_m'(1) = 0 \) whenever \( m \) and \( n \) are greater than 1. If gates in the first level have \( m \) (\( n \)) inputs, the expected controllabilities of all even (odd) numbered levels can be characterized by the function \( f_m(s) \) and that of the odd (even) levels by \( f_n(s) \). The respective fixed points \( p_m \) and \( p_n \) of the two functions \( f_m(s) \) and \( f_n(s) \) in the region \((0,1)\) are determined by \( m \) and \( n \). It is clear that if \( m = n \) then \( p_m = p_n = p \) which is in accordance with our model. If \( m \neq n \) then \( p_m \) need not equal \( p_n \).

Considering only the behaviour of controllabilities of alternate levels, as was done by Lipsky and Seth in [4], we need to use only one of the functions, \( f_n(s) \) or \( f_m(s) \) depending on whether the first level has \( n \)-input gates or \( m \)-input gates. Theorem 5c) allows us to conclude that, if the primary input controllability is different from the fixed point then as \( i \) tends to infinity the controllabilities of two consecutive levels \( i \) and \( i + 1 \) converge respectively to either 0 and 1 or 1 and 0.

6 Extensions to General NAND Circuits with Reconvergent Fanouts

The results presented up to now were based on the simplifying assumption that the circuit does not have any reconvergent fanouts. This assumption implies that the random variables representing signal values at the inputs of any gate are statistically independent. To extend our earlier results to NAND circuits with arbitrary structures would be analytically intractable. However, we can address the following simpler, and equally relevant, question. Under what conditions are the asymptotic results, presented earlier with the assumption of independence, valid in the presence of reconvergent fanouts? In this section we address this question by examining the correlation between the random variables that represent signal values on different lines that originate from a common gate.

As mentioned earlier, we model a circuit (without significant restrictions) as one with no feed-forward. Using this model, we see that if two fanout paths reconverge at a gate in level \( \ell \), then both the reconvergent lines must be in level \( \ell - 1 \). Therefore, we need to consider the correlation between lines in different fanout paths, only if the lines are in the same level.
Consider the circuit shown in Figure 5, where gate $G_1$ at level $i$, has a fanout of 2, giving rise to two paths $P_1$ and $P_2$. Let $B_j$ be a random variable representing the signal values on the output of gate $G_j$. Since the analysis of the general case of reconvergent fanouts, is intractable, we study a simple case to illustrate the behaviour of correlation between signal values on two fanout paths. We assume that, for each gate shown in the figure, the signal values on input lines that are not in the paths $P_1$ and $P_2$, are statistically independent. It seems to be intuitively clear that the correlation between signal values on a line in $P_1$ and the corresponding line in $P_2$ would decrease as the fanins of gates along $P_1$ and $P_2$ increase. Due to this reason, one would also expect this correlation to decrease, as the “distance”, of lines from the fanout stem, increases. To support these intuitive ideas, we present the following results. The proofs of some of these results are easy and are omitted from this paper.

We first define the following measure of correlation between signal values $B_{2d}$ and $B_{2d+1}$ of two gates $G_{2d}$ and $G_{2d+1}$ in the paths $P_1$ and $P_2$ respectively, at level $i + d$ (see Figure 5).

Definition: Let $x, y \in \{0, 1\}$. Then the dependence function

$$\Phi_d : \{0, 1\}^2 \rightarrow \mathbb{R}$$
such that

\[ \Phi_d(x, y) = P\{B_{2d} = x, B_{2d+1} = y\} - P\{B_{2d} = x\}P\{B_{2d+1} = y\} \]

for \( d = 1, 2, \ldots \). \( \square \)

Thus, \(|\Phi_d|\) expresses the pointwise distance between 1) the joint probability distribution function of the random variables \( B_{2d} \) and \( B_{2d+1} \) and 2) the pointwise product of the distribution functions of \( B_{2d} \) and that of \( B_{2d+1} \). In general \( \Phi \) can be defined for any two discrete random variables. Some of the properties of the dependence function are as follows.

1. \( \sum_{x,y \in \{0,1\}} |\Phi_d(x, y)| = 0 \text{ if and only if } B_{2d} \text{ and } B_{2d+1} \text{ are independent.} \) This condition holds for general discrete random variables.

2. \( \Phi_d(1,1) \) is the covariance of \( B_{2d} \) and \( B_{2d+1} \). This is true for any two 2-valued (binary) random variables.

Therefore, \( \Phi_d(x, y) \) is a more general expression for dependence between two random variables than their covariance or correlation coefficient.

Based on the above definition, we now consider the dependence between signal values \( B_2 \) and \( B_3 \) on gates \( G_2 \) and \( G_3 \) conditioned on the fanins \( k_2 \) and \( k_3 \).

**Lemma 5:** Let \( G_1 \) be at level \( i \) and let \( Y_i \) be the random variable representing controllability of a line in level \( i \). Then, under the above assumptions, \( \Phi_1 \) conditioned on \( k_2 \) and \( k_3 \) is a random variable and its expected value can be expressed in the following manner.

\[
E[\Phi_1(x, y) \mid k_2, k_3] = (-1)^{(x \oplus y)} (\mu_i)^{k_2+k_3-1} (1 - \mu_i)
\]

(19)

where \( \oplus \) denotes the EX-OR operation.

**Proof:** (see Appendix D) \( \square \)

In the following lemma, we set up a recurrence relation between expected values of \( \Phi_d \) and \( \Phi_{d-1} \) \( (d \geq 2) \) conditioned on the fanins of gates in the two paths upto level \( i + d \).
Lemma 6: Under the above assumptions

\[ E[\Phi_d(x, y) \mid k_{2j}, k_{2j+1}, j = 1, \ldots, d] = \]

\[ (-1)^{\langle x \oplus y \rangle} (\mu_{i+d-1})^{k_{2d}+k_{2d+1}-2} E[\Phi_{d-1}(1, 1) \mid k_{2j}, k_{2j+1}, j = 1, \ldots, d-1]. \]  \hspace{1cm} (20)

Proof: (see Appendix D)

This leads us to the following theorem.

Theorem 7: The joint distribution function of the two random variables \(B_{2d}\) and \(B_{2d+1}\) converges uniformly, to the product of the two distribution functions, in the limit as one or more fanins \(k_n \to \infty\) for \(2 \leq n \leq 2d + 1\).

Proof: From Lemmas 5 and 6 it follows that under the assumptions of the circuit in Figure 5,

\[ E[\Phi_d(x, y) \mid k_j, j = 2, \ldots, 2d + 1] = \]

\[ (-1)^{\langle x \oplus y \rangle} (1 - \mu_i) (\mu_i)^{k_2+k_3-1} \prod_{n=2}^{d} (\mu_{i+n-1})^{k_{2n}+k_{2n+1}-2}. \]  \hspace{1cm} (21)

From the above equation it is clear that

\[ \lim_{k_n \to \infty} E[\Phi_d(x, y) \mid k_j, j = 2, \ldots, 2d + 1] = 0 \]

for \(2 \leq n \leq 2d + 1\). This implies that the random variable \(\Phi_d(x, y)\) conditioned on \(k_n\)'s, converges to 0 for each point \((x, y) (x, y \in \{0, 1\})\). Therefore, the joint distribution function of the random variables \(B_{2d}\) and \(B_{2d+1}\) converge pointwise to the product of the two distribution functions. Further, since the joint distribution function is defined on a discrete and finite set and is bounded, pointwise convergence also implies uniform convergence. This completes the proof.

We know that if \(B_{2d}\) and \(B_{2d+1}\) were independent, their joint distribution function would be the product of the individual distribution functions. Thus, from Theorem 7 we can conclude that as the fanins of one or more of the gates in paths \(P_1\) and \(P_2\) increase, the joint distribution function of \(B_{2d}\) and \(B_{2d+1}\) approaches a function that represents the joint distribution function of the two random variables if they were independent. This allows us to conclude that the mutual dependence of the random variables \(B_{2d}\) and \(B_{2d+1}\) decreases as fanins of gates in the paths increases.
In order to determine the behaviour of the joint distribution function of $B_{2d}$ and $B_{2d+1}$ as a function of the distance $d$, of the gates $G_{2d}$ and $G_{2d+1}$ from $G_1$ (the stem), we need to remove the conditioning of the function $\Phi_d(x, y)$, on the fanins of different gates. We state without proof that the unconditional expectation of the random variable $\Phi_d(x, y)$ can be expressed as

$$E[\Phi_d(x, y)] = (-1)^{(x+y)}\mu_i (1 - \mu_i) \prod_{n=0}^{d-1} [r(\mu_{i+n})]^2$$  \hspace{1cm} (22)$$

where $r(s) = \frac{g_X(s)}{s}$. The properties of the function $r(s)$ are stated in the following proposition.

**Proposition 2:** The function $r(s)$ has the following properties.

a) Derivatives of $r(s)$ of all orders are non-negative for $s \geq 0$ and therefore $r(s)$ is increasing and convex in $[0, 1]$.

b) $r(1) = 1$ and $r(0) = \lim_{s \to 0} \frac{g_X(s)}{s} = p_1$ where $p_1$ is the probability that a gate has a fanin of 1.

**Proof:**

a) Since $g_X(s) = \sum_{k=1}^{\infty} s^k p_k$, we can see that

$$r(s) = \sum_{k=1}^{\infty} s^{k-1} p_k. \hspace{1cm} (23)$$

Denoting the $n$th derivative of $r(s)$ by $D^{(n)}(r(s))$ we obtain

$$D^{(n)}(r(s)) = \sum_{k=n-1}^{\infty} (k-1)[_n] s^{k-n-1} p_k$$

where $(k-1)[n] = \frac{(k-1)!}{(k-n-1)!}$. It is obvious from the above equation that $D^{(n)}(r(s)) \geq 0$ for $s \geq 0$.

b) This part follows directly from Equation (23). \hfill \square

Using Proposition 2 and Equation (22), we can now say that if $\mu_{i+n-1} \neq 1$, then expected value of the random variable $\Phi_d(x, y)$ converges to 0 as $d$ increases. More formally

$$\lim_{d \to \infty} E[\Phi_d(x, y)] = 0$$
for \( m \geq 1 \). This means that as the distance between lines, on two fanout paths, and their stem increases, \( \Phi_d(x, y) \) approaches the zero-valued random variable. This, as mentioned above, also implies that the joint distribution function of \( B_{2d} \) and \( B_{2d+1} \) approaches that of two independent random variables. Therefore, when distances to reconvergence are large, the assumption of independence between signal values, on different inputs of a gate, produce better approximations of the actual controllability values.

It is interesting to note that it is for these cases (i.e., when distances to reconvergence is large) that complexities for test generation as well as controllability/detectability computation (using supergates of [6] for example), is high. For such cases, the authors of [6] define a heuristic based on a threshold \( T \) of the distance between a stem and its reconvergence. The above results provide a validation of the threshold heuristic presented in [6] for computing controllabilities and detectabilities. Moreover these results can be used to define criteria for choosing a threshold.

We now address the problem of finding a suitable threshold \( T \) for a circuit such that signal values on lines which are at least a distance of \( T \) from each other have negligible dependence. We again consider the special case circuit illustrated in Figure 5. Gate \( G_1 \) is in level \( i \) of the circuit. We can restate the above problem as follows. Our aim is to determine the distance \( T \), such that signal values on lines in paths \( P_1 \) and \( P_2 \) located at levels \( T + i \) (\( i \geq 0 \)) have a dependence whose magnitude is less than a specified value \( \epsilon \). More formally, given \( \epsilon > 0 \), we want to find \( T \) such that

\[
|E[\Phi_T(x, y)]| < \epsilon.
\]

We assume that fanins of gates follow a generalized geometric distribution with parameters \( a \) and \( b \). Let us first consider the case where \( a + b < 1 \). We illustrate the method for obtaining \( T \) for the case when the level \( i \), of gate \( G_1 \) (the stem) is even and \( \mu_0 < p \). \( T \) can be obtained for other cases using similar analyses. Under the above assumptions, we know from Theorem 5 that

\[
\mu_{i+2j} < \mu_{i+2(j-1)} < \cdots < \mu_{i+2} < \mu_i < \mu_{i-2} < \cdots
\]

We obtain a bound for the expected value of \( \Phi_d(x, y) \) by considering the contribution of only the even numbered levels to the dependence function of Equation (22). Using the fact
that \( r(s) \) is increasing and \( r(s) \in [a, 1) \) for \( s \in [0, 1) \) (see Proposition 2), we get

\[
|E[\Phi_d(x, y)]| = \mu_i (1 - \mu_i) \prod_{n=0}^{d-1} [r(\mu_i + n)]^2
\]

\[
< \mu_i (1 - \mu_i) \prod_{m=0}^{[(d-1)/2]} [r(\mu_i + 2m)]^2
\]

\[
< \mu_i (1 - \mu_i) \left( [r(\mu_i)]^2 \right)^{[(d-1)/2]+1}
\]

\[
= \begin{cases} 
\mu_i (1 - \mu_i) [r(\mu_i)]^d & d \text{ even} \\
\mu_i (1 - \mu_i) [r(\mu_i)]^{d+1} & d \text{ odd.}
\end{cases}
\] (24)

Given \( \epsilon > 0 \), we can now determine \( T \) from Inequality (24) as follows.

\[
T = \left\lceil \frac{\ln \left( \frac{\epsilon}{\mu_i (1 - \mu_i)} \right)}{\ln (r(\mu_i))} \right\rceil.
\] (25)

Inequality (24) provides loose bounds on the expected value of the dependence between signal values on different lines. Thus \( T \) in the above equation provides a pessimistic upper bound on the distance between lines such that the dependence between their values is less than \( \epsilon \).

7 Controllability Characteristics in Other Reconvergence-Free Homogeneous Circuits

In this section we present, briefly, some results on controllability characterization in reconvergence-free AND, OR and NOR gate circuits. Thus our study is again restricted to gates whose inputs are statistically independent. Further, we assume that these circuits do not have any feed-forward.

Let \( Z_i \) be the random variable representing the controllability of a gate in level \( i \) of a reconvergence-free AND gate circuit. Let the number of inputs to a gate in level \( i \) be \( k \) and let the respective controllabilities at these input lines be represented by \( Z_{i-1,1} \) through \( Z_{i-1,k} \). Thus, \( k \) is a realization of the random variable \( X \) defined in Section 3. Then

\[
Z_{i|X=k} = Z_{i-1,1} Z_{i-1,2} \cdots Z_{i-1,k}.
\] (26)
We now state, without proof, the following results.

Let $\eta_i^{(m)}$ denote the $m$th moment of the random variable $Z_i$. Given that the control-
labilities of all gates in a level are iid it can be shown that $\eta_i^{(m)} = g_X(\eta_{i-1}^{(m)})$. Further, since $g_X^{(d)}(s) = g_X(g_X^{(d-1)}(s))$, we can write $\eta_i^{(m)} = g_X^{(i)}(\eta_0^{(m)})$.

It is clear that in order to characterize the limiting behaviour of controllabilities in
these circuits we need to study the properties of $g_X(s)$. Using some of these properties
discussed in Lemma 1, the following can be proven.

Let $p_1 = P\{X = 1\} < 1$. Under this condition, if $\eta_k^{(m)} = 0(1)$ for some $k \geq 0$, then
$\eta_k^{(m)} = 0(1)$ for $i \geq 0$. However, if $\eta_k^{(m)} \in (0,1)$ for some $k \geq 0$ then $\lim_{i \to \infty} \eta_k^{(m)} = 0$.

It can also be shown that the variance of $Z_i$ approaches 0 as $i$ increases. Note that
we need not place any restrictions on the distribution of $X$ to obtain the above results.
Thus, the space of circuits being considered here is the set of all reconvergence-free AND
gate circuits. Using these results, we can show that if $Z_0$ is identically equal to $q \in (0,1)$,
then $\eta_i^{(m)} (i \geq 0)$ is bounded above by $q^m$ and thus $Var(Z_i)$ is bounded above by $q^2$.

The above results constitute a stochastic characterization of controllabilities of gates
in different levels of reconvergence-free AND gate circuits.

An obvious extension to the above results is in controllability characterization of
reconvergence-free OR and NOR gate circuits. In the beginning of this paper we defined
controllability of a gate as the probability of having a logic ‘1’ at the output of that gate.
Instead we now define the probability of having a logic ‘0’ at the output of a gate as the
0-controllability of that gate.

We define the random variables $\overline{Y}_i$ and $\overline{Z}_i$ associated with gates in NOR and OR
circuits respectively to represent the probability of a gate in level $i$ to have a logic value
‘0’ (0-controllability) on it. Let $X$ represent the number of inputs to a gate in a circuit.
Consider a gate at level $i$ of a reconvergence-free circuit (either OR or NOR tree). Let the
number of inputs to this gate be $k$, i.e. $k$ is a realization of the random variable $X$. Then
we can see that

$$\overline{Y}_i \bigg|_{X=k} = 1 - \overline{Y}_{i-1,1} \overline{Y}_{i-1,2} \cdots \overline{Y}_{i-1,k}$$ (27)
\[ \bar{Z}_i |_{X=k} = \bar{Z}_{i-1,1} \bar{Z}_{i-1,2} \cdots \bar{Z}_{i-1,k} \]  \hspace{1cm} (28)

where \( \bar{Y}_{i-1,j} (\bar{Z}_{i-1,j}) \) represents the 0-controllability of input \( j \) \((j = 1 \ldots k)\) in level \( i - 1 \) of a NOR (OR) gate.

Since the expression for \( \bar{Y}_i (\bar{Z}_i) \) in terms of \( \bar{Y}_{i-1,j} (\bar{Z}_{i-1,j}) \) is exactly the same as that of \( Y_i (Z_i) \) in terms of \( Y_{i-1,j} (Z_{i-1,j}) \) (see Equations (1) and (26)), it is easy to see that under the same assumptions on the distribution of \( X \) the analysis presented for 1-controllability in reconvergence-free NAND (AND) circuits holds for 0-controllability in reconvergence-free NOR (OR) circuits.

8 Experimental and Simulation Results

In this section we present some empirical results regarding the distribution of fanins and controllability behaviour.

8.1 Empirical Evidence for Gate Fanin Distribution

The \( pmf \) of a generalized geometric distribution given by Equation (7) has two unknown parameters \( a \) and \( b \). These parameters can be estimated from circuit data by using maximum likelihood (see Appendix F). Let \( n \) be the total number of gates. Let \( r \) be the total number of gates with fanin of 1 and let \( U \) denote the total fanin of all gates with fanin greater than 1. Then the maximum likelihood estimates \( \hat{a} \) of \( a \) and \( \hat{b} \) of \( b \) are given by

\[
\hat{a} = \frac{r}{n} \hspace{1cm} (29)
\]

\[
\hat{b} = \frac{U - 2(n - r)}{U - (n - r)} \hspace{1cm} (30)
\]

The above estimators for \( a \) and \( b \) were computed for the ISCAS benchmark circuits [2]. The empirical \( pmf \) of fanins and the theoretical \( pmf \) using \( \hat{a} \) and \( \hat{b} \) are shown for four of the circuits in Figure 6. Thus, we see that the generalized geometric distribution provides a good model for describing the distribution of fanins.
Figure 6: Actual and predicted distributions for fanins of gates in four ISCAS benchmark circuits.
8.2 Controllability Behaviour

We now present some results of simulation experiments with actual circuits and compare them with theoretical predictions obtained from the analysis presented in Section 3.

NAND gate trees were generated by simulating the distribution of $X$ to yield fanins for different gates. Next we carried out true value simulations on each circuit for a large number of random input patterns. The proportion of 1's on each line $j$ at each level $i$ of the circuit was used as our observation $\hat{y}_{i,j}$ of controllability $Y_{i,j}$ of the line. We then computed the sample mean $\hat{\mu}_i^{(1)}$, of the controllabilities, using

$$\hat{\mu}_i^{(1)} = \frac{1}{n_i} \left( \sum_{j=1}^{n_i} \hat{y}_{i,j} \right)$$

(31)

where $n_i$ is the number of gates in level $i$.

$\hat{\mu}_i^{(1)}$ for different levels of two 10-level NAND gate trees is illustrated in Figure 7. The parameters of the distribution for $X$ for the first circuit are $a = 0.203902$ and $b = 0.285714$ ($n = 1589$). Parameter values for the second circuit are $a = 0.191190$ and $b = 0.418464$ ($n = 2552$).

Using these parameter values we used Equation (8) to compute theoretical predictions of expected controllability $\mu_i^{(1)}$. These are also plotted in the same figure and shows very close agreement between the theoretical predictions and actual observations.

9 Fault Observability and Fault Coverage in Reconvergence-Free NAND Gate Circuits

For reconvergence-free circuits, the set of input patterns that can detect a fault on a line is a superset of the set of patterns that detect a fault on at least one of the primary input lines. Due to this reason, a set of patterns that detect all primary input faults also detect all faults in the circuit. In this section, we consider two testability measures of reconvergence-free NAND circuits, namely 1) observability and 2) expected coverage of primary input faults.
Figure 7: Theoretical predictions and actual observations of expected controllabilities in different levels of two NAND trees.
The former metric measures the following quantity. Given that a fault effect is present at one of the primary inputs of the circuit, what is the probability that this fault effect will be observed at its primary outputs? In case the circuit being considered is part of a larger circuit, such a fault effect may be due to faults, from other sub-circuits, that have propagated to the inputs of this sub-circuit.

The latter measure is used to estimate the number of faults of the circuit that have been tested for. The assumption made here is that the primary input fault coverage is a good measure of the fault coverage in the whole circuit.

In the following sections we obtain expressions for the observability of primary input faults in general reconvergence-free NAND gate circuits. Following this we present some results on optimality of expected observability of primary input faults. Next we obtain expressions for expected fault coverage and discuss maximization of expected primary input fault coverage.

9.1 Fault Observability

Consider a fault on a primary input line that is activated and propagated to an input of a gate $g$ at level $i$. The input line is at level $i-1$. We want to find the probability $W_i$ that the fault propagates to the output of gate $g$. Let the fanin of gate $g$ be $k$ (numbered 1 through $k$). Without loss of generality assume that the fault has propagated to input $k$ of the gate, (i.e. inputs of the gate in question, can be reordered without affecting our results). $W_i$, conditioned on the fanin of the gate, is therefore

$$W_i|X=k = Y_{i-1,1}Y_{i-1,2}\cdots Y_{i-1,k-1}. \quad (32)$$

Let $V_j$ be a random variable representing the observability of a fault $F_j$ (on primary input line $j$) at a primary output. This can be extended to several primary outputs by summing the expected observabilities over all outputs. We consider only the case of a single primary output. Given a NAND circuit with $L$ levels, numbered 1 through $L$ (not including the primary inputs which are assumed to be at level 0), $V_j$ for any primary input $j$ can be expressed as

$$V_j = \prod_{i=1}^{L} W_i = V. \quad (33)$$
Since $W_i$'s are functions of fanins of gates, $V$ is also a function of fanins. Therefore, since fanin $X$ is a random variable we see that observability $V$ of a primary input is also a random variable.

**Theorem 8:** The $m$th moment of $V$ is given by

$$E[(V)^m] = \prod_{i=0}^{L-1} r\left(\mu_i^{(m)}\right). \tag{34}$$

where $r(s) = \frac{g_X(s)}{s}$.

**Proof:** (see Appendix E)

Proposition 2 (Section 6) states some of the useful properties of the function $r(s) = g_X(s)/s$. Theorem 8 characterizes the distribution of primary input observability $V$ by its moment generating function (mgf). The expression for expected primary input observability can be obtained from Equations (34) and (3) as

$$E[V] = \prod_{i=0}^{L-1} r(\mu_i) = \prod_{i=0}^{L-1} r(h^{(i)}(\mu_0)), \tag{35}$$

where $h^{(i)}(s)$ is defined as the $i$ times composition of the function $h(s)$.

We now address the problem of maximizing input fault observability. This is the same as finding the optimal weight for weighing random input patterns.

### 9.2 Optimality of Expected Observability

Given a reconvergence-free NAND circuit with $L$ levels, we want to determine the value of input controllability that maximizes input fault observability. Let $D_L(s) = r(s)r(h(s))\cdots r(h^{(L-1)}(s))$. Thus, given an $L$ level NAND circuit and a $\mu_0$, $E[V] = D_L(\mu_0)$. Let $\nu_L$ denote the value of $\mu_0$ for which the function $D_L(\mu_0)$ is maximized. For the following analysis we assume that $X$ follows a *generalized geometric distribution*.

We now present some results on determining the value of $\mu_0$ that maximizes $E[V]$. We shall consider separately, the two cases of the number of levels $L$ in the circuit, namely 1) $L$ is even and 2) $L$ is odd. We now state the following theorem.
Theorem 9: Let \( p \) be the unique fixed point of \( h(s) \) and let \( \nu_L \in [0,1] \) be such that \( D_L(\nu_L) \geq D_L(s) \) for all \( s \in [0,1] \). Then, if \( L \) is even,

\[

\nu_L = \begin{cases} 
  (0,p) & \text{when } a + b < 1 \\
  s & \forall s \in [0,1] \text{ when } a + b = 1 \\
  [p,1] & \text{when } a + b > 1
\end{cases}

\]

and if \( L \) is odd

\[

\nu_L = \begin{cases} 
  1 & \text{when } a + b = 1 \\
  [p,1] & \text{when } a + b \neq 1.
\end{cases}

\]

Proof: (see Appendix E) \( \square \)

The significance of Theorem 9 lies in the fact that it tells us which region \( \mu_0 \) should be in, for a given \( L \), so as to maximize the expected primary input observability. The following additional characteristics of the optimal point \( \nu_L \), can be observed.

Let \( p_1 \) denote the probability \( Pr\{X = 1\} \) (probability of the fanin of a gate being 1). Similarly, let \( p_2 \) denote \( Pr\{X = 2\} \). In terms of \( a \) and \( b \), \( p_1 = a \) and \( p_2 = (1 - a)(1 - b) \). When \( p_1 < p_2 \), as \( L \) increases \( \nu_L \) converges to \( p \) (from below when \( L \) is even and from above when \( L \) is odd). This occurs because, when \( p_1 < p_2 \), \( a + b < 1 \), implying (see Theorem 5) that if \( \mu_0 \neq p \), as \( L \) increases, the controllabilities of gates in successive levels degenerate to either 1 or 0. The effect of this on observability is that, as \( L \) increases, propagation of faults through alternate levels (where the expected controllabilities degenerate to 0) becomes increasingly difficult. Thus, the only way to allow a somewhat uniform propagation of faults through all levels is by setting \( \mu_0 = p \), since this would preserve the expected controllabilities of all levels at the same value.

However, when \( p_1 = p_2 \) (again \( a + b < 1 \)), the point of optimality remains constant with increase in \( L \), i.e. \( \nu_{2k+1} = \nu_1 = 1 \) and \( \nu_{2k} = \nu_2 \in (0,p] \) for all non-negative integers \( k \).

When \( p_1 > p_2 \), if \( L \) is odd \( \nu_L = 1 \). However, when \( L \) is even, three different characteristics can be observed depending on the values of \( a \) and \( b \). If \( a + b < 1 \), then as \( k \) increases \( \nu_{2k} \) converges to \( p \). When \( a + b = 1 \), then as stated in Theorem 9, every point in the interval \([0,1]\) is an optimal point. When \( a + b > 1 \) the optimal point \( \nu_L = 1 \).

We now address the problem of maximizing expected primary input fault coverage in reconvergence-free NAND circuits.
9.3 Optimization of Expected Fault Coverage

Let \( I \) be the set of primary inputs with \( |I| = N_I \). Let \( \xi_{j,v,\tau} (v \in \{0,1\}) \) be a random variable associated with the \( s-a-v \) fault on primary input \( j \) such that

\[
\xi_{j,v,\tau} = \begin{cases} 
1 & \text{\( s-a-v \) fault on line } j \text{ is detected in } \tau \text{ test cycles} \\
0 & \text{otherwise.}
\end{cases}
\]

The following results assume that there is only one primary output. For more primary outputs the results can be extended easily by summing the expected fault coverage over all the outputs. We can express the primary input fault coverage \( F_I \) as

\[
F_I = \sum_{j=1}^{N_I} (\xi_{j,1,\tau} + \xi_{j,0,\tau}) .
\]

The probability that a \( s-a-v \) fault on primary input \( j \) is detected, conditioned on the values of \( Y_0 \) and \( V \), are given below for \( v \in \{0,1\} \).

\[
P(\xi_{j,1,\tau} = 1 | V, Y_0) = 1 - (1 - (1 - Y_0)V)^\tau
\]

\[
P(\xi_{j,0,\tau} = 1 | V, Y_0) = 1 - (1 - Y_0V)^\tau
\]

Since the above probabilities are functions of the random variables \( Y_0 \) and \( V \), they are themselves random variables. We are interested in their expected values which can be expressed as

\[
E[P(\xi_{j,1,\tau} = 1 | V, Y_0)] = 1 - (1 - (1 - E[Y_0])E[V])^\tau
\]

\[
E[P(\xi_{j,0,\tau} = 1 | V, Y_0)] = 1 - (1 - E[Y_0]E[V])^\tau .
\]

This follows from the independence of \( Y_0 \) and \( V \).

We can express the expected primary input fault coverage, conditioned on the values of \( V \) and \( Y_0 \), in the following manner.

\[
E[F_I | V, Y_0] = E \left[ \sum_{j=1}^{N_I} (\xi_{j,1,\tau} | V, Y_0) + \xi_{j,0,\tau} | V, Y_0) \right]
\]

\[
= \sum_{j=1}^{N_I} (E[\xi_{j,1,\tau} | V, Y_0] + E[\xi_{j,0,\tau} | V, Y_0]) .
\]
Since $\xi_{j,0,\tau}$ are Bernoulli random variables Equation (36) can be written as

\[
E [F_I \mid V, Y_0] = \sum_{j=1}^{N_I} \left( E[P\{\xi_{j,1,\tau} = 1 \mid V, Y_0\}] + E[P\{\xi_{j,0,\tau} = 1 \mid V, Y_0\}] \right)
\]

\[
= \sum_{j=1}^{N_I} \left[ 1 - (1 - (1 - E[Y_0])E[V])^\tau \right] + \left[ 1 - (1 - E[Y_0]E[V])^\tau \right]
\]

\[
= N_I (2 - (1 - (1 - \mu_0)D_L(\mu_0))^\tau - (1 - \mu_0 D_L(\mu_0))^\tau)
\]

\[
= N_I G(\mu_0)
\]

(37)

The optimization problem, alluded to above, can now be restated as follows. Given an $L$-level reconvergence-free NAND circuit we want to determine $s_L^* \in [0,1]$ such that $G(s_L^*) \geq G(s)$ for all $s \in [0,1]$ where $G(s)$ is as defined in Equation (37). In general it is difficult to find $s_L^*$ which maximizes the function $G(s)$ for a given $L$-level circuit. Instead, we focus our attention on the limiting behaviour of $s_L^*$ as $\tau$ increases. In other words we can find an optimal weight for input random patterns so that when the number of input patterns increases the expected fault coverage is maximized. This result is stated and proved below.

**Theorem 10:** Given a reconvergence-free $L$ level NAND gate circuit, $\lim_{\tau \to \infty} s_L^* = 0.5$.

**Proof:** Taking the first derivative of $G(s)$ with respect to $s$, we get

\[
G'(s) = \tau \left[ ((1 - (1 - s)L)D_L)^{\tau-1}((1 - s)D_L'(s) - D_L(s)) \right] + \left[ (1 - s D_L)^{\tau-1}(s D_L'(s) + D_L(s)) \right].
\]

The optimal point $s_L^*$ is such that $G'(s_L^*) = 0$. The fact that $s_L^*$ is a function of $\tau$ is implicit.

Equating the above equation to 0 and performing simple manipulations, we get

\[
\left( \frac{1 - (1 - s_L^*)D_L(s_L^*)}{1 - s_L^* D_L(s_L^*)} \right)^{\tau-1} = \frac{s_L^* D_L'(s_L^*) + D_L(s_L^*)}{D_L(s_L^*) - (1 - s_L^*) D_L'(s_L^*)}
\]

\[
1 - (1 - s_L^*)D_L(s_L^*) = \left( \frac{s_L^* D_L'(s_L^*) + D_L(s_L^*)}{D_L(s_L^*) - (1 - s_L^*) D_L'(s_L^*)} \right)^{1/(\tau-1)}.
\]

From this we can see that as $\tau$ increases,

\[
\lim_{\tau \to \infty} \left( \frac{1 - (1 - s_L^*)D_L(s_L^*)}{1 - s_L^* D_L(s_L^*)} \right) = \lim_{\tau \to \infty} \left( \frac{s_L^* D_L'(s_L^*) + D_L(s_L^*)}{D_L(s_L^*) - (1 - s_L^*) D_L'(s_L^*)} \right)^{1/(\tau-1)} = 1
\]
This further implies that as $\tau$ approaches infinity $1 - s^n_L = s^n_L$ and therefore $\lim_{\tau \to \infty} s^n_L = 0.5$. This proves the theorem.

Thus, according to Theorem 10, if the number of test patterns to be applied, is sufficiently large then the expected fault coverage can be maximized by setting the primary input expected controllability $\mu_0$ to 0.5. This is a significant result since for large circuits $\tau$ is usually quite large and even if the exact $s^n_L$ for a particular (large) $\tau$ may not be determined, it can be proven (as in Theorem 10) to be sufficiently close to 0.5. Thus for large circuits, setting $\mu_0 = 0.5$ is likely to yield the high expected fault coverage. With this we conclude the analysis of observability and fault coverage in reconvergence-free NAND circuits.

10 Conclusion

In this paper, a fundamental and unique relationship, between the structure of a circuit and controllability characteristics of its gates, has been established. We consider some aggregate statistical measures of fanins and derive the relation between controllability of a gate and these statistical measures.

We presented a complete stochastic characterization for controllability behaviour in general reconvergence-free NAND circuits and provided extensions to other reconvergence-free homogeneous circuits. In the case of AND (OR) gate circuits, the results presented, hold for the complete space of reconvergence-free AND (OR) circuits, since no restriction is imposed on the distribution of fanins of gates.

In the case of reconvergence-free NAND (NOR) gate circuits, when no restriction is imposed on the distribution of gate fanins, we show that the set of levels in the circuit can be dichotomized. This partition is based on whether the expected controllabilities, within each of the two partitions, is less or greater than a certain characteristic point $p$, of the fanin distribution. We then imposed the restriction that, gate fanins follow a generalized geometric law. Experiments on benchmarks circuits were carried out and it was shown that the reduction on the size of the circuit space of practical circuits, due to this restriction, is reasonably small. We show that, under these constraints expected controllabilities in
different levels converge to one of the fixed points of a characteristic function of the fanin distribution. Further, the fixed points, that these controllabilities converge to, may vary among circuits and depends only on two parameters of the fanin distribution. Therefore, these results constitute a complete generalization of those presented in [1,4].

We have therefore, introduced the notion of a *natural classification* (by controllability values and therefore by level numbers) of gates in a rich space of reconvergence-free homogeneous circuits. The significance of the above results is due to the fact that, the reflections of structural changes on the controllability value of a gate in the circuit, can be determined easily by evaluating a simple function.

We have also stated (without proof) some results, concerning the correlation between signals on two fanout paths. It was shown that the correlation between these signal values decreases as the distance between the stem and the level of the signal increases. Our single main assumption for reconvergence-free circuits was that signals at the inputs of a gate are independent. We have shown that the above results on correlation can be used to determine criteria, under which our results on reconvergence-free circuits, are applicable to general circuits with reconvergent fanouts.

Further, we have obtained analytical expressions for the distribution of primary input fault observability. Results on determining the *weight* of signals at the primary inputs, so as to maximize the expected observability are presented. It was also shown that, the optimal weight of primary input signals, to maximize expected primary input fault coverage, approaches 0.5, as the number of test patterns increases.

Future work in this area would involve extending these models for non-homogeneous circuits. Furthermore, *the main application of controllability characterization is in testability analysis of circuits*. Thus the above results can be used in stochastic models for complete testability characterization of circuits. Work in the area of stochastic characterization of observabilities in general circuits is currently underway.

**References**


Appendix

A Proofs of Results in Section 3

Proof of Theorem 1: We can express $\mu_i^{(m)}$ as

$$\mu_i^{(m)} = E [(Y_i)^m] = E [ E [(Y_i)^m | X]].$$  \hspace{1cm} (38)

Using Equation (1) we can write $E [(Y_i)^m | X = k]$ as

$$E [(Y_i)^m | X = k] = E [(1 - Y_{i-1,1} Y_{i-1,2} \cdots Y_{i-1,k})^m]$$

$$= E \left[ \sum_{j=0}^{m} (-1)^j \binom{m}{j} (Y_{i-1,1})^j (Y_{i-1,2})^j \cdots (Y_{i-1,k})^j \right]$$

$$= \sum_{j=0}^{m} (-1)^j \binom{m}{j} E [(Y_{i-1,1})^j (Y_{i-1,2})^j \cdots (Y_{i-1,k})^j]$$

$$= \sum_{j=0}^{m} (-1)^j \binom{m}{j} E [(Y_{i-1,1})^j] E [(Y_{i-1,2})^j] \cdots E [(Y_{i-1,k})^j]$$ \hspace{1cm} (39)

$$= \sum_{j=0}^{m} (-1)^j \binom{m}{j} \left( E [(Y_{i-1})^j] \right)^k.$$ \hspace{1cm} (40)

Equations (39) and (40) follow respectively from the independence and identical distribution assumptions. Substituting Equation (40) into Equation (38) and noting that $E [(Y_{i-1})^j] = \mu_{i-1}^{(j)}$ we get

$$\mu_i^{(m)} = E \left[ \sum_{j=0}^{m} (-1)^j \binom{m}{j} \left( \mu_{i-1}^{(j)} \right)^k \right]$$

$$= \sum_{k=1}^{\infty} p_k \left[ \sum_{j=0}^{m} (-1)^j \binom{m}{j} \left( \mu_{i-1}^{(j)} \right)^k \right]$$

$$= \sum_{j=0}^{m} (-1)^j \binom{m}{j} \sum_{k=1}^{\infty} p_k \left( \mu_{i-1}^{(j)} \right)^k$$

$$= \sum_{j=0}^{m} (-1)^j \binom{m}{j} g_{X} \left( \mu_{i-1}^{(j)} \right).$$ \hspace{1cm} (41)
This proves the theorem.

Proof of Lemma 1: The proof for a) is as follows.

\[ g_X'(s) = \sum_{k=1}^{\infty} kp_k s^{k-1}. \]  

(42)

Therefore \( g_X'(s) \geq 0 \) for \( s \geq 0 \) and if \( p_1 > 0 \) then \( g_X'(s) > 0 \) for \( s \geq 0 \).

For b) we consider the second derivative of \( g_X(s) \).

\[ g_X''(s) = \sum_{k=2}^{\infty} k(k-1)p_k s^{k-2}. \]  

(43)

Therefore for \( s \in [0,1] \) \( g_X''(s) > 0 \).

The proof of part c) is as follows. For \( s = 0 \) it is easy to see that \( g_X(s) = 0 \) and for \( s = 1 \), \( g_X(1) = \sum_{i=1}^{\infty} p_i = 1 \). Therefore \( s = 0 \) and \( 1 \) are fixed points of \( g_X(s) \). To prove that \( 0 \) and \( 1 \) are the only fixed points of \( g_X(s) \) for \( s \in [0,1] \) we need to show that \( \beta \zeta \in (0,1) \) such that \( g_X(\zeta) = \zeta \). Suppose, instead, that \( \exists \zeta \in (0,1) \) such that \( g_X(\zeta) = \zeta \). Then by mean value theorem \( \exists \xi_1 \in (0,\zeta) \) and \( \exists \xi_2 \in (\zeta,1) \) such that \( \xi_1 \neq \xi_2 \) and

\[ g_X'(\xi_1) = \frac{g_X(\zeta) - g_X(0)}{\zeta - 0} = 1 \]

\[ g_X'(\xi_2) = \frac{g_X(1) - g_X(\zeta)}{1 - \zeta} = 1. \]

Since \( g_X'(s) \) is continuous, the above implies (again by mean value theorem) that there is at least one point \( \xi_3 \in (\xi_1,\xi_2) \subset (0,1) \) such that

\[ g_X''(\xi_3) = \frac{g_X'(\xi_1) - g_X'(\xi_2)}{\xi_1 - \xi_2} = 0. \]  

(44)

But this is a contradiction since in part b) above we proved that for \( s \in [0,1] \) \( g_X''(s) > 0 \). Therefore \( s = 0 \) and \( 1 \) are the only fixed points of \( g_X(s) \) in the interval \([0,1]\).

To prove d) we consider the following argument. Since by part a) \( g_X(s) \) is monotonically increasing and \( 0 \leq g_X(s) \leq 1 \) for \( s \in [0,1] \) we have \( 0 \leq h(s) \leq 1 \) and \( h(s) \) is monotonically decreasing for \( s \in [0,1] \) and continuous. Therefore the function \( e(s) = h(s) - s \) is monotonically decreasing and continuous. Further \( e(0) = 1 \) and \( e(1) = -1 \). By the intermediate
value theorem and monotonicity of \( e(s) \) there exists one and only one point \( p \in (0, 1) \) such that \( e(p) = 0 \). This implies that \( p \) is the unique fixed point of \( h(s) \).

\( \square \)

**Proof of Theorem 2:**

a) The proof of the necessary condition is as follows. Let \( q \) be a fixed point of \( f(s) \). Since \( f(s) = h(h(s)) \), this implies \( h(h(q)) = q \) and therefore, taking \( h \) of both sides, we have

\[
h(h(h(q))) = f(h(q)) = h(q).
\]

Thus, \( h(q) \) is also a fixed point of \( f(s) \). To prove the sufficient condition, we note that \( f(h(q)) = h(q) \). Restating this we can see that \( h(f(q)) = h(q) \) and therefore, taking \( h^{-1} \) of both sides (this is possible since, by Lemma 1, \( h \) is a monotonically decreasing 1-1 function), we get \( f(q) = q \).

b) Let \( p \in (0, 1) \) be the unique fixed point of \( h(s) \) (by Lemma 1d). We can say that \( p \) is also a fixed point of \( f(s) \) since

\[
f(p) = h(h(p)) = h(p) = p.
\]

Therefore \( f(s) \) has at least one fixed point in the interval \( (0, 1) \). Further

\[
f(0) = h(h(0)) = h(1) = 0 \quad \& \quad f(1) = h(h(1)) = h(0) = 1.
\]

Therefore \( s = 0 \) and \( s = 1 \) are also fixed points of \( f(s) \). Thus \( f(s) \) has at least three fixed points in the closed interval \([0, 1]\).

c)

\[
f'(s) = h'(h(s))h'(s) = g_X'(h(s))g_X'(s).
\] (45)

From Equation (45), we can see that for \( k = 1 \),

\[
(f^{(1)})'(0) = (f^{(1)})'(1) = (g_X'(1)g_X'(0)).
\]

Suppose this is true for some \( k \), then writing \( f^{(k+1)}(s) \) as \( f(f^{(k)}(s)) \) we get, using the chain rule for differentiation

\[
(f^{(k+1)})'(0) = f'(f^{(k)}(0))(f^{(k)})'(0)
\]

\[
= f'(0)(f^{(k)})'(0)
\]

\[
= f'(0)(g_X'(1)g_X'(0))^k
\]

\[
= (g_X'(1)g_X'(0))^{k+1}
\]

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Therefore the hypothesis is true for $k + 1$. By induction it is true for all $k$. Since, by Lemma 1a, $g_X'(s) \geq 0$ for all $s \in [0, 1]$, we can see that $(f^{(k)})'(s) > 0$ in this interval. This proves part b) of the theorem.

\[ \square \]

\section*{B Proofs of Results in Section 4}

\textbf{Proof of Lemma 2:} \\
a) This follows directly by substituting $a = 1 - b$ in Equation (10).

Part b) can be proved as follows. The function $f(s)$ (when $X$ follows a generalized geometric law) is given by Equation (10). In order to get the fixed points of $f(s)$ we need to get the solutions of the equation $f(s) - s = 0$. In other words we need to solve for $s$ in the equation

\[ P(s)Q(s) - sR(s) = 0. \tag{46} \]

Since $R(s)$ is a polynomial of degree 3, $sR(s)$ is a polynomial of degree 4. Similarly both $P(s)$ and $Q(s)$ are polynomials of degree 2. Thus the LHS of Equation (46) is a polynomial in $s$ of degree 4. This implies that there are at most 4 solutions to Equation (46) and consequently at most 4 fixed points for $f(s)$.

We also know from Theorem 2b) that if $\zeta$ is a fixed point of $h(s)$ it is also a fixed point of $f(s)$. It can be seen from Equation (9) that $h(s)$ has two fixed points $p, q \neq 1, 0$, of which exactly one is in the region $(0, 1)$ (by Lemma 1d)). Therefore, $p$ and $q$ are also fixed points of $f(s)$. Thus the four fixed points of $f(s)$ are $p, q, 1$ and 0. This implies $f(s)$ exactly three fixed points in the region $[0, 1]$.

\[ \square \]

\textbf{Proof of Lemma 3:} From Theorem 2c, we know that

\[ f'(0) = g_X'(0)g_X'(1) = a + \frac{a(1 - a)}{1 - b}. \]

Therefore,

\begin{align*}
  f'(0) < (\Leftarrow) [>] 1 & \iff a + \frac{a(1 - a)}{1 - b} < (\Leftarrow) [>] 1 \\
  & \iff a(1 - a) < (\Leftarrow) [>] (1 - b)(1 - a) \\
  & \iff (1 - a)(a + b - 1) < (\Leftarrow) [>] 0 \\
  & \iff (a + b - 1) < (\Leftarrow) [>] 0.
\end{align*}
The last relation follows from that fact that $0 \leq a < 1$ and therefore $(1 - a) > 0$. This proves the lemma.

**Proof of Theorem 5**: Part a) is a restatement of of Theorem 3b and needs no further proof.

For parts b) and c) we can define two sequences $\{\mu_{2i}\}$ and $\{\mu_{2i+1}\}$ for integers $i \geq 0$ such that $\mu_{2i} = f(\mu_{2(i-1)})$ and $\mu_{2i+1} = f(\mu_{2(i-1)+1})$ for integers $i \geq 1$. Further, by Theorem 2c, $f(s)$ is monotonically increasing and by Lemma 2b, $f(s)$ has exactly three fixed points in $[0,1]$, namely $s = 0, p$ and 1. Therefore we can define two intervals $I_1 = (0,p)$ and $I_2 = (p,1)$.

We now prove part b) as follows. We are given that $f'(0) > 1$. By the *corollary* to Theorem 4 $f(s) > s(< s)$ for $s \in I_1(I_2)$. If $\mu_0 \in I_1$ then, by Lemma 8 (Appendix C), the sequence $\{\mu_{2i}\}$ converges to $p$. Also in this case Theorem 3a implies that $\mu_1 \in I_2$ and therefore (again by Lemma 8 of Appendix C), the sequence $\{\mu_{2i+1}\}$ converges to $p$. Alternatively, if $\mu_0 \in I_2$ then $\mu_1 \in I_1$ (by Lemma 8), and both sequences converge to $p$. Therefore we can say that $\lim_{i \to \infty} \mu_i = p$.

Proof of part c) is as follows. We are given that $a + b < 1$. By the *corollary* to Theorem 4 $f(s) < s(> s)$ for $s \in I_1(I_2)$. If $\mu_0 < p$ (i.e. $\mu_0 \in I_1$ and therefore by Theorem 3a $\mu_1 \in I_2$) then by Lemma 8 (Appendix C), the sequence $\{\mu_{2i}\}$ converges to 0 and the sequence $\{\mu_{2i+1}\}$ converges to 1. Instead when $\mu_0 \in I_2$ (and therefore $\mu_1 \in I_1$) then, again by Lemma 8, the sequence $\{\mu_{2i}\}$ converges to 1 and the sequence $\{\mu_{2i+1}\}$ converges to 0. This proves the theorem.

**Proof of Theorem 6**: We first note that $E[(Y_i)^2] = \mu_i^{(2)} \in [0,1]$. This is true since the random variable $Y_i$ is defined on $[0,1]$. Now consider the expected controllabilities $Y_i$ and $Y_{i+1}$ of two consecutive levels $i$ and $i+1$. By Theorem 5c), it is clear that $\lim_{i \to \infty} \mu_i = 0(1)$ and $\lim_{i \to \infty} \mu_{i+1} = 1(0)$. Without loss of generality let us assume that $\lim_{i \to \infty} \mu_i = 0$ and $\lim_{i \to \infty} \mu_{i+1} = 1$. In that case, using Equation (2) to express the second moment of $Y_i$, we get

$$
\lim_{i \to \infty} \mu_{i+1}^{(2)} = 1 - 2 \lim_{i \to \infty} g_X(\mu_i) + \lim_{i \to \infty} g_X(\mu_i^{(2)})
$$

$$
= 1 - 2g_X(\lim_{i \to \infty} \mu_i) + \lim_{i \to \infty} g_X(\mu_i^{(2)})
$$

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\[ = 1 + \lim_{i \to \infty} g_X(\mu_{i+1}^{(2)}). \tag{47} \]

Since the function \( g_X(s) \in [0, 1] \) for \( s \in [0, 1] \) we can say that the RHS of Equation (47) is in the region \([1, 2]\). But \( \lim_{i \to \infty} \mu_{i+1}^{(2)} \in [0, 1] \). Therefore \( \lim_{i \to \infty} \mu_{i+1}^{(2)} = 1 \). Further, we had assumed that \( \lim_{i \to \infty} \mu_{i+1} = 1 \). By using Equation (4) we can now see that \( \text{Var}(Y_{i+1}) = 0 \). Moreover, Equation (47) and the fact that \( \lim_{i \to \infty} \mu_{i+1}^{(2)} = 1 \) imply that \( \lim_{i \to \infty} g_X(\mu_i^{(2)}) = 0 \). Since we had assumed that \( \lim_{i \to \infty} \mu_i = 0 \), we can also see that \( \text{Var}(Y_i) = 0 \). This proves the theorem.

Proof of Lemma 4: Consider Figure 4. If \( \mu_0 \leq z \), then the level \( N0(\epsilon) \), at which expected controllability is less than \( \epsilon \) can be approximated by the number of steps, of the function \( A(s) \), required to go from \( \mu_0 \) to \( \epsilon \). This is given by

\[ \left[ \log \left( \frac{\epsilon}{\mu_0} \right) / \log(f'(0)) \right]. \]

If \( \mu_0 > z \), then \( N0(\epsilon) \) can be approximated by the sum of two quantities, namely 1) the number of steps of \( B(s) \) required to go from \( \mu_0 \) to \( zf'(0) \) (see Figure 4) and 2) the number of steps of \( A(s) \) to go from \( zf'(0) \) to \( \epsilon \). This is given by

\[ \left[ \log \left( \frac{zf'(0) - \frac{\epsilon}{1-m}}{\frac{\mu_0 - \frac{\epsilon}{1-m}}{\log(m)}} \right) + \frac{\log \left( \frac{\epsilon}{\mu_0} \right)}{\log(f'(0))} \right]. \]

C Two Fixed Point Characteristics

In this appendix we prove some general analytical results that will be useful in characterizing the limiting behaviour of controllabilities in reconvergence-free NAND gate circuits.

Lemma 7: Let \( \alpha \) and \( \beta \) \((\alpha < \beta)\) be two consecutive fixed points of a continuous function \( \Theta(s) \) (i.e. there exists no other point \( \zeta \) in the interval \((\alpha, \beta)\) such that \( \Theta(\zeta) = \zeta \)). Then for the interval \( I = (\alpha, \beta) \) \( \Theta(s) < s \forall s \in I \) if and only if \( \exists \xi \in I \) such that \( \Theta(\xi) < \xi \). A similar statement can be made for \( \Theta(s) > s \forall s \in I \).

Proof: We prove only the case where \( \Theta(s) < s \forall s \in I \). The necessary condition is obvious
and needs no proof. To prove the sufficient condition consider the following argument. We are given that \(\exists \xi \in I\) such that \(\Theta(\xi) < \xi\). Assume that \(\Theta(s) \not\in s \forall s \in I\). This means \(\exists \xi_1 \in I\) such that \(\Theta(\xi_1) \geq \xi_1\). Since \(\Theta(s)\) is continuous, the function \(e(s) = \Theta(s) - s\) is also continuous. Therefore \(e(\xi) < 0\) and \(e(\xi_1) \geq 0\). Let us assume without loss of generality that \(\xi < \xi_1\). By continuity of \(e(s)\) in \(I\) and intermediate value theorem we can say that there exists at least one point \(\zeta \in [\xi, \xi_1]\) such that \(e(\zeta) = 0\). This implies that \(\Theta(\zeta) = \zeta\) for some \(\zeta \in I\). This is a contradiction. \(\Box\)

Lemma 8: Let \(\alpha\) and \(\beta\) (\(\alpha < \beta\)) be two consecutive fixed points of a continuous, monotonically increasing function \(\Theta(s)\) defined on \([\alpha, \beta]\). Let \(\{s_i\}\) (for integers \(i \geq 0\)) be a sequence of real numbers such that \(s_0 \in I = (\alpha, \beta)\) and \(s_i = \Theta(s_{i-1})\) for \(i \geq 1\). If \(\Theta(s) < s\) (\(\Theta(s) > s\)) for \(s \in I\), then the sequence \(\{s_i\}\) converges and \(\lim_{i \to \infty} s_i = \alpha\) (\(\lim_{i \to \infty} s_i = \beta\)).

Proof: We first need to prove that the sequence \(\{s_i\}\) is well defined, i.e. since \(s_i = \Theta(s_{i-1})\) we have to show that \(s_i \in [\alpha, \beta]\) for all integers \(i \geq 0\). Suppose this is not true. Then there exists \(j \geq 1\) such that either \(s_j < \alpha\) or \(s_j > \beta\) and \(s_i \in [\alpha, \beta]\) for \(0 \leq i < j\). Note that, by assumption \(s_0 \in I\). If \(s_j < \alpha\) (\(s_j > \beta\)), since \(\Theta(s)\) is continuous in \(I\), by mean value theorem there exists at least one point \(\zeta \in (\alpha, s_{j-1})\) (\(\zeta \in (s_{j-1}, \beta)\)) such that

\[
\Theta'(\zeta) = \frac{\Theta(s_{j-1}) - \Theta(\alpha)}{s_{j-1} - \alpha} = \frac{s_j - \alpha}{s_{j-1} - \alpha} < 0 \quad (\Theta'(\zeta) = \frac{\Theta(\beta) - \Theta(s_{j-1})}{\beta - s_{j-1}} = \frac{\beta - s_j}{\beta - s_{j-1}} < 0).
\]

(48)

This is a contradiction since by assumption \(\Theta(s)\) is monotonically increasing.

Let \(\Theta(s) < s\) (\(\Theta(s) > s\)) for \(s \in I\). Then \(s_i = \Theta(s_{i-1}) < s_{i-1}\) (\(s_i = \Theta(s_{i-1}) > s_{i-1}\)). Thus the sequence \(\{s_i\}\) is monotonically decreasing (increasing). Further \(\{s_i\}\) is bounded below (above) by \(\alpha\) (\(\beta\)), since otherwise by the same argument in the previous paragraph we can find a point \(\zeta\) in some subinterval of \(I\) where \(\Theta'(\zeta) < 0\). Thus by monotonicity and boundedness of \(\{s_i\}\) the sequence converges.

To prove that the limit of \(\{s_i\}\) is \(\alpha\) (\(\beta\)) when \(\Theta(s) < s\) (\(\Theta(s) > s\)), we consider the following argument. Let \(\xi\) be the limit of \(\{s_i\}\). Surely \(\alpha \leq \xi < s_0\) (\(s_0 < \xi \leq \beta\)). Further, since \(\xi\) is the limit we have \(\Theta(\xi) = \xi\). Therefore \(\xi < s_0\) (\(\xi > s_0\)) and \(\xi\) is a fixed point of \(\Theta(s)\). This implies that \(\xi = \alpha\) (\(\xi = \beta\)) since the only fixed point in the interval \([\alpha, s_0]\) \((s_0, \beta)\) is \(\alpha\) (\(\beta\)). This proves the lemma. \(\Box\)
D Proofs of Results in Section 6

Proof of Lemma 5: We prove this only for the case when \( x = y = 1 \). The other cases can be proved in a similar manner.

\[
\Phi_1(1, 1 | k_2, k_3) = P\{B_2 = 1, B_3 = 1\} - P\{B_2 = 1\}P\{B_3 = 1\}.
\]

Assume the inputs to the gates \( G_2 \) and \( G_3 \) are numbered such that the output of gate \( G_1 \) is numbered 1 for both gates. Let \( y_{j,k} \) denotes the controllability of the \( k \)th input of gate \( G_j \). Under the assumption that the other inputs to the two gates are statistically independent and noting that \( y_{2,1} = y_{3,1} \), the first term in the RHS of the above equation, conditioned on the values \( y_{j,k} \), can be written as

\[
P\{B_2 = 1, B_3 = 1\} = (1 - y_{2,1}) + y_{2,1}(1 - y_{2,2} \times y_{2,3} \times \cdots \times y_{2,k_2})(1 - y_{3,2} \times y_{3,3} \times \cdots \times y_{3,k_3})
\]

Similarly, the second term can be written as

\[
P\{B_2 = 1\}P\{B_3 = 1\} = (1 - y_{2,1} \times y_{2,2} \times \cdots \times y_{2,k_2})(1 - y_{3,1} \times y_{3,2} \times \cdots \times y_{3,k_3})
\]

But, by assumption, each \( y_{j,k} \) is an independent realization of the random variable \( Y_i \) representing controllability values of lines in level \( i \). Skipping some algebraic details, we can now express the expected value of \( \Phi_d(x, y) \) as

\[
E[\Phi_1(1, 1) | k_2, k_3] = (E[Y_i])^{k_2+k_3-1} - (E[Y_i])^{k_2+k_3}
\]

\[
= (\mu_i)^{k_2+k_3-1} (1 - \mu_i)
\]

\[
= (-1)^{(1\oplus 1)} (\mu_i)^{k_2+k_3-1} (1 - \mu_i).
\]

\( \square \)

Proof of Lemma 6: We use induction to prove this only for the case when \( x = y = 1 \). Let \( d = 2 \).

\[
\Phi_2(1, 1 | k_{2j}, k_{2j+1}, j = 1, 2) =
\]

\[
P\{B_4 = 1, B_5 = 1 | k_{2j}, k_{2j+1}, j = 1, 2\} - P\{B_4 = 1 | k_{2j}, j = 1, 2\}P\{B_5 = 1 | k_{2j+1}, j = 1, 2\}.
\]

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Using the independence of controllability values at different inputs, the above equation can be simplified and expressed as

\[
E[\Phi_2(1, 1) | k_{2j}, k_{2j+1}, j = 1, 2] = \\
\left[ 1 - (\mu_{i+1})^{k_4-1} \right] \left[ 1 - (\mu_{i+1})^{k_5-1} \right] E[\Phi_1(1, 1)|k_2, k_3] + \\
\left[ 1 - (\mu_{i+1})^{k_4-1} \right] E[\Phi_1(0, 1)|k_2, k_3] + \\
\left[ 1 - (\mu_{i+1})^{k_5-1} \right] E[\Phi_1(0, 1)|k_2, k_3] + \\
E[\Phi_1(0, 0)|k_2, k_3]
\]

\[
= E[(\Phi_1(1, 1))|k_2, k_3] (\mu_{i+1})^{k_4+k_5-2}
\]

(49)

The last equation follows from the fact that the expected value of \( \Phi_1(x, y) \) conditioned on \( k_2 \) and \( k_3 \), can be written as

\[
E[\Phi_1(x, y)|k_2, k_3] = (-1)^{(x \oplus y)}E[\Phi_1(1, 1)|k_2, k_3]
\]

as shown in Lemma 5. Thus we see that the hypothesis of Equation (21) holds for \( d = 2 \). Equation (49) forms the basis for our induction. Suppose this holds for \( d = n \). We need to show that it holds for \( d = n + 1 \). \( \Phi_{n+1}(1, 1) \) conditioned on \( k_{2j} \) and \( k_{2j+1} \) for \( j = 1 \) to \( n + 1 \) can be expressed as

\[
E[\Phi_{n+1}(1, 1) | k_{2j}, k_{2j+1}, 1 \leq j \leq n + 1] = \\
\left[ 1 - (\mu_{i+n})^{k_{2(n+2)}-1} \right] \left[ 1 - (\mu_{i+n})^{k_{2(n+2)}-1} \right] E[\Phi_n(1, 1)|k_{2j}, k_{2j+1}, 1 \leq j \leq n] + \\
\left[ 1 - (\mu_{i+n})^{k_{2(n+2)}-1} \right] E[\Phi_n(1, 0)|k_{2j}, k_{2j+1}, 1 \leq j \leq n] + \\
\left[ 1 - (\mu_{i+n})^{k_{2(n+2)}-1} \right] E[\Phi_n(0, 1)|k_{2j}, k_{2j+1}, 1 \leq j \leq n] + \\
E[\Phi_n(0, 0)|k_{2j}, k_{2j+1}, 1 \leq j \leq n]
\]

\[
= E[\Phi_n(1, 1)|k_{2j}, k_{2j+1}, 1 \leq j \leq n] (\mu_{i+n})^{k_{2(n+2)}+k_{2(n+2)}-2}
\]

The last equation follows from the fact that

\[
E[\Phi_n(x, y)|k_{2j}, k_{2j+1}, 1 \leq j \leq n] = (-1)^{(x \oplus y)}E[\Phi_n(1, 1)|k_{2j}, k_{2j+1}, 1 \leq j \leq n].
\]

Thus we see that the hypothesis holds for \( d = n + 1 \) and therefore holds for all \( d \).  

\[ \square \]
E Proofs of Results in Section 8

Proof of Theorem 8: It is easy to show that $W_i$ and $W_j$ ($i \neq j$) depend on different sets of primary inputs and therefore they are independent random variables. Using this fact and Equation (33), we can say that

$$E[(V)^m] = E \left[ \left( \prod_{i=1}^{L} W_i \right)^m \right]$$

$$= \prod_{i=1}^{L} E[(W_i)^m].$$

(50)

We now use Equation (32) to obtain the expression for $E[(W_i)^m]$.

$$E[(W_i)^m] = E [E [(W_i)^m \mid X = k]]$$

$$= \sum_{k=1}^{\infty} E [(W_i)^m \mid X = k] P\{X = k\}$$

$$= \sum_{k=1}^{\infty} E [(Y_{i-1,1} Y_{i-1,2} \cdots Y_{i-1,k-1})^m] P\{X = k\}$$

(51)

Since the random variables $Y_{i-1,j}$ are independent and identically distributed, Equation (51) can be written as

$$E[(W_i)^m] = \sum_{k=1}^{\infty} (E [(Y_{i-1})^m])^{k-1} P\{X = k\}$$

$$= \sum_{k=1}^{\infty} (\mu_{i-1}^{(m)})^{k-1} P\{X = k\}$$

$$= \frac{1}{\mu_{i-1}} \sum_{k=1}^{\infty} (\mu_{i-1}^{(m)})^k P\{X = k\}$$

$$= \frac{1}{\mu_{i-1}} g_X(\mu_{i-1}^{(m)}) = r(\mu_{i-1}^{(m)})$$

(52)

(53)
Using Equations (50) and (52), we get

\[ E[(V)^m] = \prod_{i=1}^{L} r\left(\frac{\mu_{i-1}^{(m)}}{\mu_{i-1}^{(m)}}\right) = \prod_{i=0}^{L-1} r\left(\frac{\mu_{i}^{(m)}}{\mu_{i}^{(m)}}\right) \]  

(54)

This completes the proof. \qed

**Lemma 9:** Let \( X \) follow a generalized geometric distribution with \( a + b < 1 \), \( a \neq 1 \) and \( b \neq 1 \). Then \( D_L' (0) > 0 \) for any \( L \geq 1 \).

**Proof:** We know that \( r(s) = \sum_{k=1}^{\infty} s^{k-1} p_k \). Therefore, \( r'(0) = p_2 \) and

\[ r'(1) = \sum_{k=1}^{\infty} (k-1) p_k = \sum_{k=1}^{\infty} k p_k - \sum_{k=1}^{\infty} p_k = E[X] - 1. \]

We can see easily that the above hypothesis is true for \( L = 1 \) since \( D_1(s) = r(s) \) and \( r'(0) = p_2 > 0 \). Let \( L = 2 \). Then \( D_2(s) = r(s)r(h(s)) \). Therefore

\[ D'_2(0) = r'(0)r(h(0)) + r(0)r'(h(0))h'(0) = r'(0)r(1) - r(0)r'(1)g'_X(0). \]

Further \( g'_X(0) = p_1 \). Using these relations and Proposition 2, we get

\[ D'_2(0) = p_2 - (p_1)^2 (E[X] - 1). \]  

(55)

Since \( X \) follows a generalized geometric distribution, we have from Equations (7) and (11) that 1) \( p_1 = a \), 2) \( p_2 = (1-a)(1-b) \) and 3) \( E[X] - 1 = \frac{1-a}{1-b} \). Using these facts we can rewrite Equation (55) as

\[ D'_2(0) = \frac{1-a}{1-b} (1 - (b-a))(1 - (a+b)) \]

Since \( a + b < 1 \), this implies that \( b - a < 1 \) and therefore from the above equation, \( D'_2(0) > 0 \).

Suppose this is true for \( L = 2k \) for some integer \( k \). Then we can express \( D_{2k+1}(s) \) and \( D_{2k+2} \) as follows (we state these without proof).

\[ D_{2k+1}(s) = D_{2k}(s) \times r \left( f^{(k)}(s) \right) \]

\[ D_{2k+2}(s) = D_{2k}(s) \times r \left( f^{(k)}(s) \right) \times r \left( f^{(k)}(h(s)) \right) \]
It is easy to show that $D'_{2k+1}(0) > 0$. This is done as follows.

$$
D'_{2k+1}(0) = D'_{2k}(0)r\left(f^{(k)}(0)\right) + D_{2k}(0)r'\left(f^{(k)}(0)\right)\left(f^{(k)}\right)'(0)
$$

$$
= D'_{2k}(0)r(0) + D_{2k}(0)r'(0)\left(f^{(k)}\right)'(0)
$$

$$
> 0. \quad (56)
$$

Equation (56) follows from the fact that $f^{(k)}(0) = 0$ for all integers $k \geq 0$. Inequality (57) is true because by hypothesis $D'_{2k}(0) > 0$ and therefore, by Proposition 2 and Theorem 2c, every term on the RHS of Equation (56) is positive.

To prove that $D'_{2k+2}(0) > 0$ we express $D'_{2k+2}(0)$ in terms of $a$ and $b$. Skipping some of the algebraic details, we can express $D'_{2k+2}(0)$ as

$$
D'_{2k+2}(0) = p_1D'_{2k}(0) + D_{2k}(0)\left[r'(0)\left(f^{(k)}\right)'(0) - (p_1)^2r'(1)\left(f^{(k)}\right)'(1)\right]
$$

$$
= p_1D'_{2k}(0) + D_{2k}(0)\left[f^{(k)}\right]'(0)\left[r'(0) - (p_1)^2r'(1)\right] \quad (58)
$$

Equation (58) follows directly from Theorem 2c. We can simplify this equation further and get

$$
D'_{2k+2}(0) = p_1D'_{2k}(0) + D_{2k}(0)\left(\frac{1-a}{1-b}\right)(1-(b-a))\left(1-(a+b)\right)\left(f^{(k)}\right)'(0). \quad (59)
$$

Since $a + b < 1$ and $D'_{2k}(0) > 0$ (by hypothesis), we can see that $D'_{2k+2}(0) > 0$. Thus by induction the hypothesis holds for all $k > 1$ or in other words for all $L \geq 1$. This proves the lemma.

**Proof of Theorem 9:** We only prove this for the case when $L$ is even.

Let $a + b < 1$ and $L = 2k$ for some positive integer $k$. We show that for any $\zeta \in (p, 1)$ there exists $0 < \zeta \leq p$ such that $D_L(\zeta) > D_L(\zeta)$. Next we show that $\nu_L \neq 1, 0$. Thus we prove that $\nu_L$ must be in $(0, p]$

Let $\zeta \in (p, 1)$. Consider the set of expected controllabilities in successive levels of a reconvergence-free NAND circuit starting with $\mu_0 = \zeta$. This set is $\{\zeta, h(\zeta), h^{(2)}(\zeta), \ldots, h^{(L-1)}(\zeta)\}$ Thus

$$
D_L(\zeta) = r(\zeta) \times r(h(\zeta)) \times r(h^{(2)}(\zeta)) \times \cdots \times r(h^{(L-1)}(\zeta)). \quad (60)
$$
Now set $\zeta = h[-1](\zeta)$. It is clear that $\zeta$ is well defined (because $h(s)$ is monotonically decreasing). Further, since by assumption $1 > \zeta > p$, by Theorem 3a, it is clear that $0 < \zeta < p$. Given that $h^{(i)}(h^{-1}(s)) = h^{(i-1)}(s)$, we can see that

$$D_L(\zeta) = r(h^{(-1)}(\zeta)) \times r(\zeta) \times r(h(\zeta)) \times \cdots \times r(h^{(L-3)}(\zeta)) \times r(h^{(L-2)}(\zeta)).$$  

(61)

Comparing Equations (60) and (61) we can see that

$$\frac{D_L(\zeta)}{D_L(\zeta)} = \frac{r(h^{(L-1)}(\zeta))}{r(h^{(-1)}(\zeta))}.$$

To prove that $D_L(\zeta) < D_L(\zeta)$, it is enough to show that $r(h^{(L-1)}(\zeta)) < r(h^{(-1)}(\zeta))$. Further, since by Proposition 2, $r(s)$ is monotonically increasing, the last condition implies that it is enough to show that $h^{(L-1)}(\zeta) < h^{(-1)}(\zeta)$. Since $h(s)$ is monotonically decreasing, this condition translates to showing that $h(h^{(L-1)}(\zeta)) > h(h^{(-1)}(\zeta))$. But, if $L = 2k$, then $h(h^{(L-1)}(\zeta)) = f^{(k)}(\zeta)$ and $h(h^{(-1)}(\zeta)) = \zeta$. Theorem 5c tells us that when $a + b < 1$ $\zeta < f^{(k)}(\zeta)$.

This implies that if $L$ is even for any $\zeta \in (p, 1)$, there exists a $\zeta \in (0, p]$ such that $D_L(\zeta) > D_L(\zeta)$. Therefore $\nu_L$ cannot lie in the interval $(p, 1)$.

We now show that $\nu_L \neq 1, 0$. From Lemma 9 we know that $D_L(0) > 0$. Thus there exists at least one point $\zeta > 0$ such that $D_L(\zeta) > D_L(0)$. Therefore, $\nu_L > 0$ and by definition $D(\nu_L) > D_L(0)$. Furthermore, when $L = 2k$, $D_L(1) = D_L(0) = (p_1)^k$. This also implies that $D(\nu_L) > D_L(1)$ and therefore $\nu_L \neq 1$. We have thus proven that when $L$ is even and $a + b < 1$ $\nu_L$ cannot lie in the interval $(p, 1) \cup \{0\}$. Thus $\nu_L \in (0, p]$.

When $a + b = 1$, the corollary to Theorem 4 says that $f(s) = s$ for all $s \in [0, 1]$. Thus, it is easy to see that if $L = 2k$, then $D_L(s) = [r(s)r(h(s))]^k$. Using Equation (8) and substituting $(1 - b)$ for $a$ we get $r(s) = \frac{1 - b}{1 - bs}$, $h(s) = \frac{1 - s}{1 - bs}$ and $r(h(s)) = 1 - bs$. Thus $r(s)r(h(s)) = 1 - b$ and $D_L(s) = (1 - b)^k$. From this we see that observability, in this case, is independent of $s$.

When $a + b > 1$, then select $\zeta \in (0, p)$ and set $\zeta = h^{(-1)}(\zeta)$. By Theorem 3a, $\zeta \in [p, 1]$. Now we can use the same arguments, as in the case when $a + b < 1$, to show that $D_L(\zeta) < D_L(\zeta)$.
Thus, \( \nu_L \) cannot be in the interval \((0, p)\). Further, since \( D_L(0) = D_L(1) \) when \( L \) is even, we can see that if \( \nu_L = 0 \) then \( \nu_L = 1 \) and therefore it is enough to say that \( \nu_L \in [p, 1] \).

When \( L \) is odd, and \( a + b \neq 1 \) we can use similar arguments to prove the claims. When \( a + b = 1 \), it is easy to see that if \( L = 2k + 1 \) for some non-negative integer \( k \), then

\[
D_L(s) = [r(s)r(h(s))]^k r(s) = \frac{(1 - b)^{k+1}}{1 - bs}.
\]

This function can be shown to be monotonically increasing in the interval \([0,1]\) and therefore \( D_L(1) \geq D_L(s) \) for all \( s \in [0,1] \). Thus \( \nu_L = 1 \) in this case.

This completes the proof.  

\[ \square \]

**F Estimation of Parameters for Generalized Geometric Distribution**

Given a circuit, let \( n \) be the total number of gates and let \( r \) be the number of gates with fanin of one. The gates are numbered 1 through \( n \) with respective fanins \( f_1 \) through \( f_n \). Since the order of gates is immaterial, we let those gates with fanin greater than one be numbered 1 through \( n - r \). The likelihood function, denoted by \( L(a, b, n, r) \) of fanin distribution is given by

\[
L(a, b, n, r) = \prod_{i=1}^{n} P\{X = f_i\} = (a)^r (1 - a)^{n-r} (1 - b)^{n-r} b^C
\]

where \( C = (\sum_{i=1}^{n-r} f_i) - 2(n - r) \).

**Estimating \( \hat{a} \)**

In order to obtain the maximum likelihood estimate \( \hat{a} \) of \( a \) we need to solve the following equation for \( a \).

\[
\frac{\partial L(a, b, n, r)}{\partial a} = (1 - b)^{n-r} b^C \left[ a^{r-1}(1 - a)^{n-r-1} \{r(1 - a) - (n - r)a\} \right] = 0
\]

The solutions for \( \hat{a} \) are

\[
\hat{a} = 0, \ 1, \ \frac{r}{n}.
\]
We need only consider the solution \( \hat{a} = r/n \) where the likelihood function has a maximum since \( \frac{\partial L(a, b, n, r)}{\partial a} \bigg|_{a=r/n} < 0 \). It can be further verified that the likelihood function has minima at \( a = 0 \) and at \( a = 1 \).

**Estimating \( \hat{b} \)**

A similar method is used to obtain an estimate \( \hat{b} \) of \( b \). The equation we need to solve for \( b \) is

\[
\frac{\partial L(a, b, n, r)}{\partial b} = a^r (1-a)^{n-r} \left[ b^{C-1} (1-b)^{n-r-1} \{ C(1-b) - (n-r)b \} \right] = 0. \tag{65}
\]

The solutions for \( \hat{b} \) are

\[
\hat{b} = 0, \ 1, \ \frac{C}{C + n - r}. \tag{66}
\]

It can be verified easily that \( L(a, b, n, r) \) has minima at \( b = 0 \) and \( b = 1 \) and has a maximum at

\[
b = \frac{C}{C + n - r} = \frac{\left( \sum_{i=1}^{n-r} f_i \right) - 2(n-r)}{\left( \sum_{i=1}^{n-r} f_i \right) - (n-r)} = \hat{b}. \tag{67}
\]
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