WIRE DELAY ESTIMATION

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Abstract

It is known that the finite resistance and capacitance associated with wire material causes a certain amount of delay in signal propagation. In this research, our goal was to find a probabilistic distribution of wire delay, prior to physical design. Predicting wiring delays in VLSI designs is of great importance, especially in submicron technology. It helps designers avoiding erroneous decisions, which could result in unsuccessful designs. Here a delay-distribution model, which gives us the probability of finding the delay less than a specified value is presented.

First of all a very simple analytical model for wiring delay, given the wire length, was validated by performing some representative SPICE experiments. We preferred this model over other existing more sophisticated models because estimates within desirable limits were achieved with this computationally simple model. Then the delay-distribution model was developed by combining the above mentioned wire-delay model with a wire-length distribution function. Other relevant statistical information like average wiring delay can also be computed with this delay-distribution function.

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1 Introduction

The finite resistance and capacitance associated with interconnect causes a certain amount of signal propagation delay. The estimation of this delay is our concern for this task. In the following section some preliminary work related to estimation of wire lengths is summarized. Then a probabilistic wire delay model based on circuit parameters is presented. Section 5 gives some SPICE simulation results. Based on these results modified models are presented. We then describe how to include the effect of contacts and bends in wires. Finally, in Section 6 we present a brief description of the software program which computes the average delay and also gives the probabilistic delay distribution. Appendices 1-4 give sample SPICE files with the MOS models used in our simulations.

2 Wire Length Estimation

To estimate wire delays we require the resistance and the capacitance of the wire and in order to know those we need the wire length. Much research has already been performed on distribution of wire lengths in VLSI chips. For our purpose the model presented in [3] is sufficient. This model is described below.

It has been shown in [1], [3] that if wire length L is a random variable with a probability distribution function $p_L(l) = P_r\{L = l\}$ then $p_L(l)$ can be assumed to be *geometric*. Sastry [3] proved that in the limiting case of optimal placements in the continuous domain the exponential distribution is the "ideal" distribution. As the geometric distribution is the discrete counterpart of the exponential distribution, we assume that $p_L(l)$ is a *geometric distribution*. Thus,

$$p_L(l) = p\,q^{l-1} \tag{1}$$

where $\frac{1}{p}$ = average wire length and $q = 1 - p$.

This distribution gives the probability of having a wire of length l, when the average wire length is $\frac{1}{p}$.

3 The Wiring Delay Model

T. Sakurai concluded in [2] that the wiring delay can be estimated by the following relationship:

$$t_{0.9} = 1.02RC + 2.21(C_tR_t + C_tR + CR_t) \tag{2}$$

where R = total resistance of the wiring,

C = total capacitance of the wiring,

C_t = load capacitance, and

R_t = equivalent resistance of the driving transistor.

To calculate R, C, R_t and C_t we require some parameters. These parameters are to be provided by the user:

r = resistance of wiring per unit length,

c = capacitance of wiring per unit length,

l = length of wiring,

r_t = sheet resistance of driving transistor when ON,

W_d =width of driving transistor,

L_d = length of driving transistor,

c_{t_i} = gate capacitance per unit area of load transistor i,

W_i =width of load transistor i, and

L_i =length of load transistor i.

From these parameters R, C, R_t and C_t can be calculated as follows:

$$R = r.l \tag{3}$$

$$C = c.l \tag{4}$$

$$R_t = r_t.\frac{L_d}{W_d} \tag{5}$$

$$C_t = \sum_{i=1}^{k} c_{t_i}.W_i.L_i, k = fanout \tag{6}$$

All these parameters depend heavily on the design and fabrication process and therefore are determined by the user.

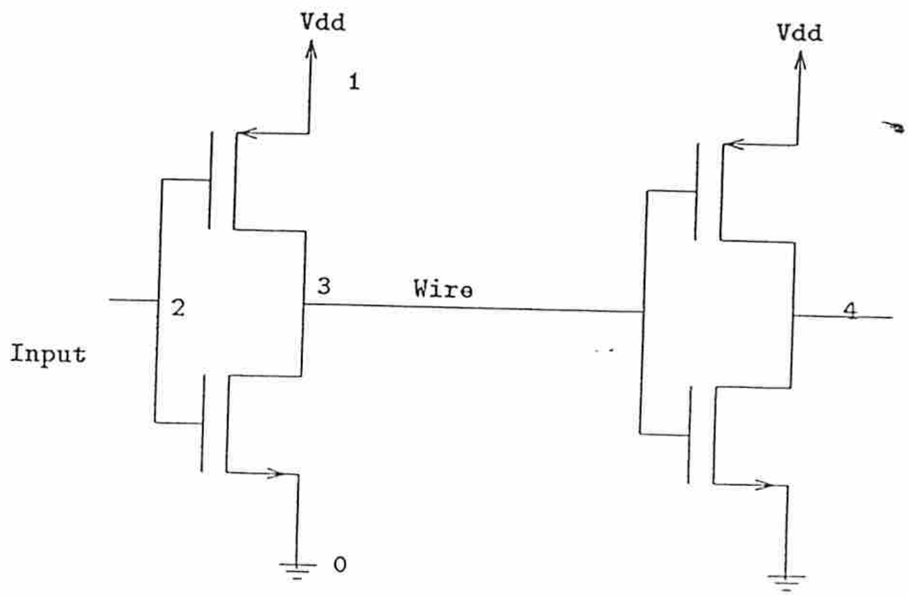

Figure 1: CMOS inverter with a fan-out of 1

For metal wiring the wire resistance is very low compared to R_t; we can assume wire-resistance $R \approx 0$. Therefore Equation(2) reduces to

$$t_{0.9} = 2.21 R_t (C_t + C) \quad (7)$$

For poly-lines R is quite high and it reduces the effect of R_t.

Parameters in the model suggested by [2] were modified based on the SPICE-simulation results.

4 Wiring delay distribution

The wire delay model can be used to derive the wire delay distribution from the length distribution curve. Let $P(T = t) = p_T(t)$ be the probability density distribution for the wire delay. Then by combining (1)and (7):

$$l = \frac{t}{ckR_t} - \frac{C_t}{c}$$

where $k = 2.21$ and l is the wire length.

$$p_T(t) = p\,q^{\left(\frac{t}{ckR_t} - \frac{C_t}{c} - 1\right)} \quad (8)$$

where, $t = kR_t \cdot (c + C_t), kR_t \cdot (2c + C_t), \ldots, \infty$

$$= p \cdot q^{-\left(\frac{C_t}{c}+1\right)} \cdot \left(q^{\frac{1}{ckR_t}}\right)^t$$

$$= RS^t \quad (9)$$

where, $R = p \cdot q^{-\left(\frac{C_t}{c}+1\right)}$ and $S = q^{\frac{1}{ckR_t}}$

This is a power series probability distribution and defines the wiring delay probability density function. The average wire delay t_{av} is computed as follows :

$$t_{av} = \sum_{t=kR_t\cdot(c+C_t)}^{\infty} t \cdot p_T(t) \quad (10)$$

$$= \sum_{t'=1}^{\infty}(kR_t \cdot (t'c + C_t)pq^{t'-1}$$

$$= kR_tC_t + kR_tc(1/p)$$

$$= kR_t(C_t + cl_{av}) \qquad \text{as } 1/p \text{ is average wire length} \quad (11)$$

5 Simulation results

Some experimental SPICE simulations were performed to verify the model. For the equivalent SPICE circuit, the metal wire was replaced by an equivalent capacitance as suggested in [2]. These experiments were performed with different types of technologies in order to make the program more versatile. The technologies considered were 1.2, 1.6, 2.0 and 3.0 micron. In all the simulations 3λ wide metal wire routing is assumed, where $\lambda = 0.6, 0.8, 1.0$ and 1.5 microns for $1.2, 1.6, 2.0$ and 3.0 micron technologies respectively. Most of the parameters in any technology are process dependent. Therefore, the model parameters may require some minor modifications when a different process is to be used.

Our experiments mostly dealt with the charging of the load capacitance rather than discharge because a PMOS transistor with equal W/L ratio is much slower than its counterpart NMOS transistor and therefore, charging takes more time more than discharging. However, generally the transistors are sized in such a way that the rise and the fall times are equal.

Simulation 1: 1.2 micron (charging).
Parameters used:

Sheet-resistance (metal)	$= 54\ mili-\Omega/\square$
Sheet-resistance (poly)	$= 28,000\ mili-\Omega/\square$
Capacitance (metal)	$= 40\ atto-farads\ /\ \mu m^2$
Capacitance (poly)	$= 68\ atto-farads\ /\ \mu m^2$
Channel resistance (p-channel)	$= 29\ K\Omega/\square$
Channel resistance (n-channel)	$= 10\ K\Omega/\square$

A sample SPICE file with the MOS models used is given in Appendix 1. The models were obtained from USC Information Sciences Institute's MOSIS Service (ISI) and SPICE3 was used to simulate these circuits.

No.	Wire Length μm	Wire Resistance Ω	Wire Capacitance fF	Fan-out	Delay Estimated ns	Delay SPICE ns
1	100	3.0	7.2	1	0.46	0.57
2				2	0.69	0.78
3				3	0.92	1.03
4	200	6.0	14.4	1	0.69	0.78
5				2	0.92	0.98
6				3	1.15	1.25
7	350	10.5	25.2	1	1.04	1.08
8				2	1.27	1.30
9				3	1.50	1.55
10	500	15.0	36.0	1	1.38	1.38
11				2	1.61	1.62
12				3	1.84	1.85
13	750	22.5	54.0	1	1.96	1.88
14				2	2.19	2.12
15				3	2.42	2.38
16	1000	30.0	72.0	1	2.54	2.42
17				2	2.77	2.63
18				3	3.00	2.88
19	1250	37.5	90.0	1	3.12	2.93
20				2	3.35	3.15
21				3	3.58	3.38
22	1500	45.0	108.0	1	3.70	3.45
23				2	3.93	3.68
24				3	4.16	3.88
25	2000	60.0	144.0	1	4.85	4.48
26				2	5.08	4.68
27				3	5.32	5.00

TABLE 1 1.2 microns charging

Simulation 2: 1.6 micron (charging).

Parameters used:

Sheet-resistance (metal)	$= 45\ mili-\Omega/\square$
Sheet-resistance (poly)	$= 26,000\ mili-\Omega/\square$
Capacitance (metal)	$= 32\ atto-farads\ /\ \mu m^2$
Capacitance (poly)	$= 65\ atto-farads\ /\ \mu m^2$
Channel resistance (p-channel)	$= 26\ K\Omega/\square$
Channel resistance (n-channel)	$= 10\ K\Omega/\square$

Appendix 2 gives a sample SPICE deck with 1.6 micron MOS models. These models were obtained from ISI and SPICE3 was used for simulation.

No.	Wire Length μm	Wire Resistance Ω	Wire Capacitance fF	Fan-out	Delay Estimated ns	Delay SPICE ns
1	100	1.875	7.68	1	0.53	0.72
2				2	0.85	1.08
3				3	1.16	1.42
4	200	3.750	15.36	1	0.76	0.92
5				2	1.07	1.26
6				3	1.38	1.605
7	350	6.5	26.88	1	1.09	1.17
8				2	1.40	1.525
9				3	1.72	1.88
10	500	9.375	38.40	1	1.42	1.44
11				2	1.73	1.785
12				3	2.05	2.155
13	750	14.00	57.6	1	1.97	1.885
14				2	2.28	2.238
15				3	2.60	2.58
16	1000	18.75	76.8	1	2.52	2.32
17				2	2.84	2.67
18				3	3.15	3.053
19	1250	23.44	96.00	1	3.07	2.79
20				2	3.39	3.11
21				3	3.70	3.46
22	1500	28.125	115.2	1	3.63	3.20
23				2	3.94	3.558
24				3	4.26	3.95
25	2000	37.5	153.6	1	4.73	4.1
26				2	5.05	4.458
27				3	5.36	4.80

TABLE 2 1.6 microns charging

Simulation 3: 2.0 micron (charging).

Parameters used:

Sheet-resistance (metal)	$= 105\ mili-\Omega/\square$
Sheet-resistance (poly)	$= 22,000\ mili-\Omega/\square$
Capacitance (metal)	$= 27\ atto-farads\ /\ \mu m^2$
Capacitance (poly)	$= 39\ atto-farads\ /\ \mu m^2$
Channel resistance (p-channel)	$= 26\ K\Omega/\square$
Channel resistance (n-channel)	$= 11\ K\Omega/\square$

Please refer to Appendix 3 for a sample SPICE file and 2.0 micron MOS models.

No.	Wire Length μm	Wire Resistance Ω	Wire Capacitance fF	Fan-out	Delay	
					Estimated ns	SPICE ns
1	100	3.5	8.1	1	0.53	0.74
2				2	0.83	1.13
3				3	1.17	1.42
4	500	17.5	40.5	1	1.46	1.51
5				2	1.76	1.88
6				3	2.06	2.25
7	750	26.25	60.75	1	2.04	2.00
8				2	2.34	2.35
9				3	2.64	2.73
10	1000	35.00	81.00	1	2.63	2.50
11				2	2.93	2.85
12				3	3.22	3.23
13	1250	43.75	101.25	1	3.21	3.00
14				2	3.51	3.35
15				3	3.81	3.72
16	1500	52.50	121.5	1	3.80	3.5
17				2	4.09	3.85
18				3	4.39	4.2
19	2000	70.00	162.00	1	4.96	4.5
20				2	5.06	4.85
21				3	5.56	5.2

TABLE 3 2micron

Simulation 4: 3.0 micron (charging).

Parameters used:

Sheet-resistance (metal)	$= 105\ mili-\Omega/\square$
Sheet-resistance (poly)	$= 30,000\ mili-\Omega/\square$
Capacitance (metal)	$= 10\ atto-farads\ /\ \mu m^2$
Capacitance (poly)	$= 19\ atto-farads\ /\ \mu m^2$
Channel resistance (p-channel)	$= 42\ K\Omega/\square$
Channel resistance (n-channel)	$= 12\ K\Omega/\square$

Appendix 4 gives a sample SPICE file with the MOS models used.

No.	Wire Length μm	Wire Resistance Ω	Wire Capacitance fF	Fan-out	Delay Estimated ns	Delay SPICE ns
1	100	2.33	4.40	1	1.07	1.38
2				2	1.93	2.27
3				3	2.80	3.15
4	200	4.66	8.80	1	1.27	1.53
5				2	2.14	2.45
6				3	3.00	3.30
7	350	8.17	15.40	1	1.58	1.75
8				2	2.45	2.65
9				3	3.31	3.57
10	500	11.67	22.00	1	1.89	2.00
11				2	2.75	2.88
12				3	3.62	3.73
13	750	17.5	33.00	1	2.40	2.36
14				2	3.26	3.23
15				3	4.13	4.08
16	1000	23.33	44.00	1	2.91	2.70
17				2	3.77	3.60
18				3	4.64	4.45
19	1250	29.17	55.00	1	3.42	3.08
20				2	4.29	3.95
21				3	5.15	4.80
22	1500	35.00	66.00	1	3.93	3.45
23				2	4.80	4.30
24				3	5.66	5.15
25	2000	46.67	88.00	1	4.96	4.15
26				2	5.82	5.00
27				3	6.69	5.85

TABLE 4 3 microns charging

6 The wiring delay software

The delay software "*wire_delay*" requires as inputs the feature size of the technology being used, the wiring material and the average wire length. It is parameterized for all the other required values. However, the user can overwrite those values and specify them for his own technology. The program computes the average delay and also generates the delay distribution as explained in the earlier sections. The distribution can be plotted in MATLAB using the post-processor software "*wire_delay.m*". A copy of all the relevant information is maintained in "*wire_delay.log*".

7 Conclusions

Depending on the technology being used we might need to adjust constants in the delay equations, as was shown in our experiments. Nevertheless, once modified, these simple relationships give us very good delay estimation given the abstract information about the design.

References

[1] F.J.Kurdahi and A.C.Parker. Techniques for Area Estimation of VLSI Layouts. *IEEE Tran. Computer-Aided Design*, 4(4):81–92, Jan 1985.

[2] T. Sakurai. Approximation of Wiring Delay in MOSFET LSI. *IEEE J. Solid-State Circuits*, SC-18(4):418–426, August 1983.

[3] S. Sastry. *Wireability Analysis of Integrated Circuits.* PhD thesis, Univ. of Southern California, January 1985.

```
*************************************************************************
*                        APPENDIX 1
*             1.2 Micron --  (CHARGING)  Model from ISI
*************************************************************************
VDD 1 0 5V
VNN 100 0 0V
*The n-substrate is tied to ground.
VPP 99 1 0V
*The p-substrate is tied to Vdd.
VIN 2 0 PULSE(5V 0V 0NS .01NS .01NS 5NS 10NS)
*************************************************************************
.model hp_pm1_du1 pmos level=4
+ vfb = -.3551 lvfb = .135058 wvfb = -0.0052928
+ phi = .729815 lphi = 0 wphi = 0
+ k1 = .621727 lk1 = -.19309 wk1 = 0.0613674
+ k2 = 0.0240414 lk2 = -0.025241 wk2 = 0.00333943
+ eta = -0.012099 leta = 0.0231103 weta = 0.0108469
+ muz = 169.689 dl = .168463 dw = .552225
+ u0 = .141719 lu0 = 0.063645 wu0 = -0.080152
+ u1 = -0.0044427 lu1 = .11348 wu1 = 0.00304771
+ x2mz = 8.07376 lx2mz = -1.5774 wx2mz = 3.43963
+ x2e = 6.03986e-05 lx2e = -0.0010498 wx2e = -0.0022319
+ x3e = 0.002712 lx3e = -0.0024406 wx3e = -0.0033537
+ x2u0 = 0.00778681 lx2u0 = -0.0010883 wx2u0 = 0.00480484
+ x2u1 = -0.0025428 lx2u1 = 0.00343822 wx2u1 = 0.00767061
+ mus = 182.561 lmus = 56.9299 wmus = -16.01
+ x2ms = 6.99205 lx2ms = 1.51385 wx2ms = 8.12972
+ x3ms = .298858 lx3ms = 3.03499 wx3ms = -1.7044
+ x3u1 = -0.012127 lx3u1 = 0.00219769 wx3u1 = -0.002664
+ tox = 0.0208 temp = 27 vdd = 5
```

```
+ cgdo = 2.09757e-10 cgso = 2.09757e-10 cgbo = 6.68072e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 119.9 cj = 0.0005316 cjsw = 2.97e-10
+ js = 1e-08 pb = .8 pbsw = .8
+ mj = .5542 mjsw = .675 wdf = 0
+ dell = 0
************************************************************************
.model hp_nm1_du1 nmos level=4
+ vfb = -1.0651 lvfb = -0.064573 wvfb = .144922
+ phi = .828744 lphi = 0 wphi = 0
+ k1 = 1.20127 lk1 = 0.0768668 wk1 = -.11886
+ k2 = .166135 lk2 = 0.0688807 wk2 = -0.080785
+ eta = -0.0095908 leta = 0.0119502 weta = 0.0229579
+ muz = 491.011 dl = .422498 dw = .345515
+ u0 = 0.0615556 lu0 = .107717 wu0 = -0.010009
+ u1 = 0.0731493 lu1 = .144105 wu1 = -.12367
+ x2mz = 1.62533 lx2mz = -2.7175 wx2mz = 44.6594
+ x2e = -0.0022784 lx2e = -0.0048768 wx2e = 0.00314731
+ x3e = 0.00168708 lx3e = -0.0014009 wx3e = -0.0082181
+ x2u0 = -0.0051476 lx2u0 = 0.000456907 wx2u0 = 0.0346245
+ x2u1 = -0.010867 lx2u1 = 0.0081172 wx2u1 = 0.00876478
+ mus = 606.502 lmus = 102.126 wmus = -155.4
+ x2ms = -9.8609 lx2ms = 9.55776 wx2ms = 65.8933
+ x3ms = 12.1792 lx3ms = 19.1536 wx3ms = -27.832
+ x3u1 = 0.0191716 lx3u1 = 0.00866737 wx3u1 = -0.022381
+ tox = 0.0208 temp = 27 vdd = 5
+ cgdo = 5.26062e-10 cgso = 5.26062e-10 cgbo = 6.02592e-10
```

```
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 95.65 cj = 0.0003116 cjsw = 8.095e-10
+ js = 1e-08 pb = .8 pbsw = .8
+ mj = 1.0364 mjsw = .1617 wdf = 0
+ dell = 0
************************************************************************
M1 3 2 1 99 hp_pm1_du1 L=1.2U W=2.4U
M2 3 2 0 100 hp_nm1_du1 L=1.2U W=1.2U
M31 4 3 1 99 hp_pm1_du1 L=1.2U W=2.4U
M41 4 3 0 100 hp_nm1_du1 L=1.2U W=1.2U
M32 4 3 1 99 hp_pm1_du1 L=1.2U W=2.4U
M42 4 3 0 100 hp_nm1_du1 L=1.2U W=1.2U
*Fan out is 2.
C1 3 0 36F
*C1 is equivalent capacitance for 500 um long metal wire.
.TRAN .05NS 5NS
.PRINT TRAN V(2,0)  V(3,0)
.END
```

```
************************************************************************
*                    APPENDIX  2
*              1.6 Micron --  (CHARGING)  Model from ISI
************************************************************************
VDD 1 0 5V
VNN 100 0 0V
*The n-substrate is tied to ground.
VPP 99 1 0V
*The p-substrate is tied to Vdd.
VIN 2 0 PULSE(5V 0V 0NS .01NS .01NS 5NS 10NS)
************************************************************************
.model imp_c1201_pm1_du2 pmos level=4
+ vfb = -.63057 lvfb = .414725 wvfb = 0.0542379
+ phi = .723555 lphi = 0 wphi = 0
+ k1 = .976346 lk1 = -.53214 wk1 = .107611
+ k2 = .110396 lk2 = -0.084891 wk2 = -0.010947
+ eta = -0.0037147 leta = 0.0329467 weta = -0.0029441
+ muz = 183.551 dl = .557873 dw = .882733
+ u0 = .150658 lu0 = 0.0421865 wu0 = -0.083566
+ u1 = -0.0073929 lu1 = .143323 wu1 = -0.028694
+ x2mz = 8.87776 lx2mz = -3.4707 wx2mz = 3.01663
+ x2e = 0.000646628 lx2e = -0.0032036 wx2e = -0.0017781
+ x3e = -0.00037459 lx3e = -0.00054927 wx3e = -0.0016729
+ x2u0 = 0.0077131 lx2u0 = -0.0033389 wx2u0 = 0.00361166
+ x2u1 = -0.0011886 lx2u1 = 0.00377034 wx2u1 = 0.00514486
+ mus = 215.435 lmus = 72.9889 wmus = -36.681
+ x2ms = 10.7984 lx2ms = -2.0802 wx2ms = 6.40887
+ x3ms = .699628 lx3ms = 7.15817 wx3ms = -3.2549
+ x3u1 = -0.0091927 lx3u1 = 0.00361721 wx3u1 = -0.0011904
+ tox = 0.0241 temp = 27 vdd = 5
```

```
+ cgdo = 5.99507e-10 cgso = 5.99507e-10 cgbo = 9.04545e-10
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 71.6 cj = 0.00047898 cjsw = 3.2291e-10
+ js = 0 pb = .85 pbsw = .85
+ mj = .485 mjsw = .3334 wdf = 0
+ dell = 0
**********************************************************************
.model imp_c1201_nm1_du1 nmos level=4
+ vfb = -.74712 lvfb = -0.066047 wvfb = 0.0518266
+ phi = .800029 lphi = 0 wphi = 0
+ k1 = .982919 lk1 = 0.0319935 wk1 = .125347
+ k2 = .152508 lk2 = 0.0713638 wk2 = -0.051424
+ eta = -0.0029668 leta = 0.0219973 weta = -0.013931
+ muz = 495.961 dl = .775241 dw = .717236
+ u0 = 0.0622543 lu0 = 0.0629245 wu0 = -0.070463
+ u1 = 0.0529802 lu1 = .277912 wu1 = -0.042678
+ x2mz = 6.36455 lx2mz = -5.6331 wx2mz = 2.94768
+ x2e = -3.6905e-05 lx2e = -0.0074159 wx2e = -0.0024452
+ x3e = 0.00072785 lx3e = -0.0017986 wx3e = -0.0023744
+ x2u0 = 0.00172426 lx2u0 = -0.0026473 wx2u0 = -0.00073041
+ x2u1 = -0.013683 lx2u1 = 0.017999 wx2u1 = 0.00856978
+ mus = 558.801 lmus = 206.669 wmus = -19.742
+ x2ms = -5.9743 lx2ms = 17.1867 wx2ms = 7.32039
+ x3ms = 2.33675 lx3ms = 34.2781 wx3ms = -4.507
+ x3u1 = 0.00772941 lx3u1 = 0.0239414 wx3u1 = -0.0067712
+ tox = 0.0241 temp = 27 vdd = 5
+ cgdo = 8.33097e-10 cgso = 8.33097e-10 cgbo = 8.54293e-10
```

```
+ xpart = 1
+ n0 = 1 ln0 = 0 wn0 = 0
+ nb = 0 lnb = 0 wnb = 0
+ nd = 0 lnd = 0 wnd = 0
+ rsh = 27.3 cj = 0.00018972 cjsw = 4.0915e-10
+ js = 1e-08 pb = .8 pbsw = .8
+ mj = .5707 mjsw = .3035 wdf = 0
+ dell = 0
************************************************************************
M1 3 2 1 99 imp_c1201_pm1_du2 L=1.6U W=3.2U
M2 3 2 0 100  imp_c1201_nm1_du1 L=1.6U W=1.6U
M31 4 3 1 99 imp_c1201_pm1_du2 L=1.6U W=3.2U
M41 4 3 0 100  imp_c1201_nm1_du1 L=1.6U W=1.6U
M32 4 3 1 99 imp_c1201_pm1_du2 L=1.6U W=3.2U
M42 4 3 0 100  imp_c1201_nm1_du1 L=1.6U W=1.6U
M33 4 3 1 99 imp_c1201_pm1_du2 L=1.6U W=3.2U
M43 4 3 0 100  imp_c1201_nm1_du1 L=1.6U W=1.6U
*Fan out is 3.
C1 3 0 76.8F
*C1 is equivalent capacitance for 1000 um long metal wire.
.TRAN 0.025NS 5NS
.PRINT TRAN V(2,0)  V(3,0)
.END
```

```
**************************************************************************
*                    APPENDIX  3
*               2 Micron --  (CHARGING)  Model from ISI
**************************************************************************
VDD 1 0 5V
VNN 100 0 0V
*The n-substrate is tied to ground.
VPP 99 1 0V
*The p-substrate is tied to Vdd.
VIN 2 0 PULSE(5V 0V 0NS 0NS 0NS 50S 100NS)
**************************************************************************
.MODEL CMOSN NMOS LEVEL=2 LD=0.208764U TOX=401.000000E-10
+ NSUB=6.422000E+15 VTO=0.754546 KP=4.821000E-05 GAMMA=0.5362
+ PHI=0.6 UO=559.83 UEXP=0.146612 UCRIT=71923.1
+ DELTA=0.506803 VMAX=66354.9 XJ=0.250000U LAMBDA=3.191846E-02
+ NFS=3.809939E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
+ RSH=24.580000 CGDO=2.696604E-10 CGSO=2.696604E-10 CGBO=7.785437E-10
+ CJ=1.085700E-04 MJ=0.682400 CJSW=5.505200E-10 MJSW=0.279800 PB=0.8
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.87 um
**************************************************************************
.MODEL CMOSP PMOS LEVEL=2 LD=0.250000U TOX=401.000000E-10
+ NSUB=6.836200E+15 VTO=-0.763626 KP=1.960000E-05 GAMMA=0.5532
+ PHI=0.6 UO=227.571 UEXP=0.290331 UCRIT=47609.9
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.050000U LAMBDA=5.341623E-02
+ NFS=2.775963E+11 NEFF=1.001 NSS=1.000000E+12 TPG=-1.000000
+ RSH=103.700000 CGDO=3.229249E-10 CGSO=3.229249E-10 CGBO=6.058196E-10
+ CJ=2.515600E-04 MJ=0.552500 CJSW=3.333800E-10 MJSW=0.337600 PB=0.8
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 0.08 um
```

```
***********************************************************************
M1 3 2 1 99 CMOSP L=2.0U W=4.0U
M2 3 2 0 100 CMOSN L=2.0U W=2.0U
M31 4 3 1 99 CMOSP L=2.0U W=4.0U
M41 4 3 0 100 CMOSN L=2.0U W=2.0U
M32 4 3 1 99 CMOSP L=2.0U W=4.0U
M42 4 3 0 100 CMOSN L=2.0U W=2.0U
M33 4 3 1 99 CMOSP L=2.0U W=4.0U
M43 4 3 0 100 CMOSN L=2.0U W=2.0U
*Fan out is 3.
C1 3 0 81F
*C1 is equivalent capacitance for 1000 um long metal wire.
.TRAN .05NS 10NS
.PRINT TRAN V(2,0)  V(3,0)
.END
```

```
*************************************************************************
* APPENDIX  4
*                 3.0 Micron -- (CHARGING)
*************************************************************************
VDD 1 0 5V
VNN 100 0 0V
*The n-substrate is tied to ground.
VPP 99 1 0V
*The p-substrate is tied to Vdd.
VIN 2 0 PULSE(5V 0V 0NS .01NS .01NS 50NS 100NS)
*************************************************************************
.MODEL CMOSP PMOS LEVEL=2 LD=0.280000U TOX=510.000E-10
+NSUB=4.012077E+14 VTO=-0.754274 KP=1.342340E-05 GAMMA=0.705848
+PHI=0.600000 UO=100.000 UEXP=0.139572 UCRIT=10000.0
+DELTA=2.35927 VMAX=100000. XJ=0.400000U LAMBDA=4.720485E-02
+NFS=1.404551E+12 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=-1.00000
+RSH=55 CGSO=4E-10 CGDO=4E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
*************************************************************************
.MODEL CMOSN NMOS LEVEL=2 LD=0.100000U TOX=500.000E-10
+NSUB=1.000000E+16 VTO=0.884599 KP=4.163698E-05 GAMMA=1.49569
+PHI=0.600000 UO=200.000 UEXP=1.001000E-03 UCRIT=999000.
+DELTA=1.05750 VMAX=48267.7 XJ=0.100000U LAMBDA=7.923688E-03
+NFS=1.239917E+12 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=1.00000
+RSH=25 CGSO=5.2E-10 CGDO=5.2E-10 CJ=3.2E-4 MJ=0.5 CJSW=9E-10 MJSW=0.33
*************************************************************************
M1 3 2 1 99 CMOSP L=3.0U W=6.0U
M2 3 2 0 100 CMOSN L=3.0U W=3.0U
M31 4 3 1 99 CMOSP L=3.0U W=6.0U
M41 4 3 0 100 CMOSN L=3.0U W=3.0U
M32 4 3 1 99 CMOSP L=3.0U W=6.0U
```

```
M42 4 3 0 100 CMOSN L=3.0U W=3.0U
M33 4 3 1 99 CMOSP L=3.0U W=6.0U
M43 4 3 0 100 CMOSN L=3.0U W=3.0U
*Fan out is 3.
C1 3 0 33F
*C1 is equivalent capacitance for 750 um long metal wire.
.TRAN 0.05NS 7NS
.PRINT TRAN V(2,0) V(3,0)
.END
```