Architecture and Routability Analysis For Row-Based FPGAs

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Abstract

FPGAs combine the logic integration benefits of custom VLSI with the design, production, and time-to-market advantages of standard logic ICs. The Actel family of FPGAs exemplifies the row-based FPGA model. Rows of logic cells interspersed with routing channels have given this family of FPGA devices the flavor of traditional channeled gate arrays or standard cells. However, unlike the conventional standard cell design, the FPGA routing channels contain predefined wiring segments of various lengths which are interconnected using antifuses. This paper develops analytical models that permit the design of FPGA routing channels and the analysis of the routability of row-based FPGAs devices based on a generic characterization of the row-based FPGA routing algorithms. In particular, it demonstrates that (using probabilistic models for the origination point and length for connections) an FPGA with properly designed segment length and distribution can be nearly as efficient as a mask-programmable channel (in terms of number of required tracks). Experimental results corroborate this prediction. In addition, this paper provides a method for evaluating various channel architectures.

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1 Introduction

1.1 Motivation

Field Programmable Gate Arrays (FPGAs) are ASICs that can be configured by the user. They combine the logic integration benefits of custom VLSI with the design, production, and time-to-market advantages of standard logic ICs. Designers define the logic functions of the circuit and revise these functions as necessary. Unlike gate arrays, standard cells and custom ICs, programmable logic devices require non-recurring costs and no custom factory fabrication.

The latest wave of FPGAs combines capabilities till now unique to gate arrays and design benefits till now found only in the programmable-array logic. These devices split broadly into two groups with different levels of granularity – that is, the size of their basic electronic structures varies. Some chips have large logic structures; the Logic Cell Array (LCA) from Xilinx Inc., consists of I/O blocks surrounding configurable logic blocks (CLBs), with each CLB including Flip-flops as well as combinational logic. Other chips resemble conventional gate arrays in their granularity; the Act 1 FPGA from Actel Corp., comprises a matrix of logic modules, with the rows separated by wiring channels. The Actel architecture is based on the antifuse technology where logic gates and their interconnections are programmed by shorting wire segments in prescribed locations.

The Actel family of FPGAs exemplifies the standard cell based FPGA model. The Actel implementation combines the advantage of mask programmable gate arrays with the flexibility of user programming. Rows of logic cells interspersed with routing channels have given the Actel architecture the flavor of traditional channeled gate arrays or standard cells. Unlike traditional gate arrays, the routing channels are not empty areas where customized metallization can be performed. Instead they contain predefined wiring segments of various lengths. These wiring segments are interconnected using a two terminal programmable element called antifuse which represents a one-time programmable element comprising of a diffusion layer placed over polysilicon with a dielectric between them. The antifuse plays the role of a via in this FPGA. There are two types of antifuses: horizontal and vertical. Horizontal fuses are used to realize longer segments by linking two adjacent horizontal segments within a channel. Vertical or cross fuses establish the link between a horizontal segment and an intersecting vertical segment which connects the routing segment on the channel to the pin on the logic block.

The segmented channel routing problem can be formulated as assigning segments to nets so as to complete all connections within the given routing resources (tracks and fuses). The foremost objective is to achieve %100 routability, secondly to minimize the number of fuses traversed by each net so as to optimize the timing characteristics. The channel segmentation design problem is to design an arrangement of segments in routing channels which is as efficient as possible. A well designed channel segment architecture should be as efficient as a non-segmented(mask programmed) routing channel in terms of number of tracks required.

There is a substantial need for studying the channel segmentation design problem for row-based FPGAs. Routing in FPGA is performed by programming the switch elements. These switches have high resistance and capacitance. Thus, the number of such switches used in routing a net should be minimized. At the same time, fewer switches imply reduced routability. Formally we can distinguish between two types of routing, i.e. one-segmented routing versus M-segmented routing.

In one-segmented routing, no horizontal fuse is allowed between two segments. In M-segmented routing, at most M adjacent segments can be connected together and this corresponds to $M-1$ horizontal fuses.

Dealing with row-based FPGAs inherently involves the problem of estimating the number of necessary tracks where tracks are straight sections of wire that span the entire width (or length) of a routing channel and can be composed of a number of wire segments of different length. The limited size of the chip constrains the number of available tracks and this can severely affect the reconfigurability of the logic blocks; so it is extremely important to have accurate estimates of the number of necessary tracks in order to decide how many and what size devices should be used to implement a given logic circuit. In addition, the delay contributed by the programmable interconnect is much higher than that of regular interconnect, and thus, the interconnection length in FPGA devices strongly influences the performance of the circuit.

1.2 Prior Work

The mask-programmable interconnect provides complete freedom for assigning a connection to any routing track while occupying only a portion of the track equal to the length of the connection plus the design rule spacing. The routing estimation and analysis problems for the customized interconnect has been researched for many years. We give a short review of the important works in this area.

Sastry and Parker [10] modeled interconnections as independent two-point wires covering an average length and derived expressions for channel widths, probability of routing completion, and wire lengths. They showed that wire length distribution has the form of a Weibull distribution with location and shape parameters. Kurdahi and Parker [7] assumed *birth* of a wire at pin slot i and length of a wire l are independent random variables with probabilities $p_B(i)$ and $p_L(l)$. They used uniform distribution for $p_B(i)$ and geometric distribution for $p_L(l)$. Based on these assumptions, the required routing area is estimated.

Sechen [11] presented an interconnection length estimator for sea-of-gates layout style. For each size of net, the half perimeter of the smallest rectangle enclosing all pins on the net is computed by assuming that a sample cell is placed randomly within a square array of area equal to the average number of its neighboring cells. Various scenarios and a look up table are used to determine all possible arrangements of cells which establish a given bounding box. Total interconnection length is then computed by summing (over all nets) the half perimeter lengths of the rectangles enclosing pins on the nets. Chen and Bushnell [3] introduced an area estimator for random placement with the assumption that wires do not share tracks. Pedram and Preas [8] presented formulas for calculating the total interconnection length and the chip height for standard cell layouts based on the notion of net neighborhood populations (that captures the competition among nets for routing resources). Their wire length model relies on knowledge of the actual design processes (placement, global routing and detailed routing), and physical structures.

The newest generation of Xilinx devices (XC4000) has provided much more routing flexibility and hence the routability analysis problem for these devices is not that much different from that of the channeled gate arrays. A routing estimation procedure for the previous generation (XC3000) is given in [1]. We therefore focus on the Actel architecture.

Traditional channel routing cannot be directly applied to row-based FPGAs since it does not take into account the restricted nature of the wiring sources. The following conceptual differences can be recognized: While in channel routing two nets can be assigned the same track if their horizontal spans do not overlap, in case of segmented channel routing each net has to be assigned to a different segment, making the channel density a function of the the particular distribution of segment lengths. In gate arrays the inputs can be assumed to be available simultaneously in both adjacent channels. For FPGAs the inputs are accessible from either the above or below channel but not both. This relaxes the problem of vertical constraints since at most one terminal enters the channel at any given column. More details on the architecture for row-based FPGAs and the segmented channel model can be found in [4] and [6], respectively.

New routing estimation and analysis procedures are needed to capture the above differences. This is a very recent development and research is therefore ongoing at different places. In the following, we review some of the relevant work.

A special case of the routing estimation for the segmented channels is addressed by El Gamal et al. [5] who showed that (in their own words) with judiciously chosen segment lengths, the channel width needed to achieve high probability of routing completion is not much greater than that for a comparable size gate array. Their assumptions are that the connection lengths are selected independently with geometrically distributed lengths and that the origination points have uniform distribution. They introduced a segmentation model in which the channel is partitioned into several regions and each region consists of tracks of equal length segments but segment length is varied uniformly across the regions. Each region is allocated certain number of tracks however the segments are not arranged in a uniform way but in a staggered fashion (see section 2 for details). This model is refered to as the **staggered non-uniform segmentation model.**

Burman et al. [2] use the staggered non-uniform segmentation model. To optimize the use of this model they propose a routing scheme based on the assignments of the nets to the appropriate track by delay computation and delay matching techniques. They determine the three parameters for this model (that is, the number of regions, the number of tracks; and the offset factor) by performing empirical analysis on several standard benchmarks.

Zhu et al. [12] describe a few shortcomings of the staggered non-uniform segmentation model and make suggestions as to how to rearrange the segment lengths in order to avoid excessive waste of segments allocated to nets in each length range and minimize the number of track types and how to scale up or down the number of tracks set aside for nets within a specific range. They also describe an algorithm that takes an arbitrary net distribution and an integer M as inputs and generates a segmented channel which is suitable for M-segment channel routing.

In the present paper, we present a generic solution to the segmentation design problem which can be tuned to any particular distribution of the connections. This is particularly important if we take into consideration the fact that various types of circuits should be mapped into different channel architectures in order to achieve higher routability. Our analytic derivations rely on a procedural characterization of the segmented routing algorithms and hence can be tuned as new algorithms replace the older generation. In contrast to the previous work, our derivations enable us to assess the appropriateness of existing architectures for various application types as shown in section 4.

1.3 Overview

In this paper, we develop models that enable us to analyze the design of segmented channel architecture as well as to study the routability problem. We adopt the staggered non-uniform segmentation model. Given the probability density functions for the origination point and length of the connections within the segmented channel, we calculate the expected number of segmented tracks of type k [1] and hence the total number of segmented tracks. If the channel segmentation architecture is not fixed, we can use this information to allocate the desired number of tracks of type k. Alternatively, if the channel architecture is fixed and the total number of tracks T is known, we can use this information to predict the probability of routing completion and if successful routing is possible, the number and types of tracks used. We have derived expressions for generic one-segmented and two-segmented routing procedures. Our approach is, however, general and can be applied to other (performance-driven) segmented routing schemes. Finally, we present closed-form expressions for the above parameters assuming specific (but prevalent) density functions for the signal origination point and length. Our models deal with one- and two-segmented routing which can be generalized to M-segmented routing as well.

The remainder of the paper is organized as follows. Section 2 contains our detailed analysis and derivations for one- and two-segmented routing paradigms. Sections 3 and 4 specialize the general results to two common special cases and describe an important application. Section 5 presents the results of our implementations. Based on our derivations, we show that up to %83 of channels generated according to our scheme are successfully routed with random input data . Section 6 presents some discussions and the ongoing work.

2 Determination of the Segmented Track Requirements

The architecture for row-based FPGAs is described in [4] and the segmented channel model is described in [6].

The following sections describe analytic derivations of the segment lengths and distributions under one-segmented and two-segmented routing models. We have assumed generic routing algorithms which choose the shortest segments at the first available track for completing connections. This model is consistent with the way most segmented routers operate.

2.1 Channel Architecture Model

We will use the following notation: L denotes the number of columns in the channel and N denotes the total number of connections in the channel. The origination point of a connection is wherever a horizontal segment is to be connected to a vertical segment and its concentration along the length of the channel may varies depending on the specific application. We assume the concentration of the origination points is either given by a histogram or certain features of it follow a special pattern. In this way we can regard the origination point as a random variable with a probability density function $f(x)$; the domain of $f(x)$ is $[0, L]$ where L is the total channel length. When a logic cell

[1] A segmented track of type k contains segments of length equal to some function of k.

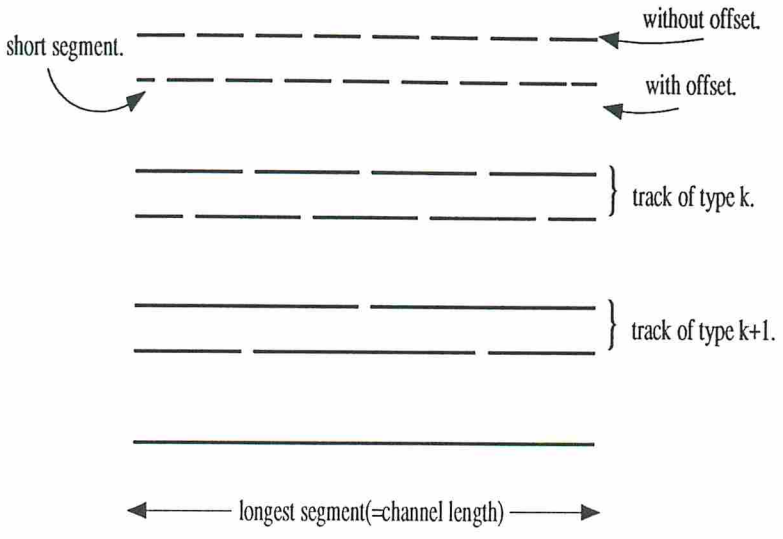

Figure 1: The FPGA Routing Channel

is to be connected to another one, depending on their physical location a certain length along the channel is to be traversed. We assume that the length of a connection is a random variable with a probability density function $h(y)$; the domain of $h(y)$ is $[0, L]$. Using the information hidden in f and h, we can predict the required number of tracks for successful routing or evaluate different architectures from a routing capability point of view.

Our formulation is general and holds for arbitrary f and h. The distributions of origination point f and connection length h greatly affect the estimations and hence the necessity for a realistic choice of f and h is of great importance. If f and h are not analytically known, we can fit curves on their corresponding histograms and treat them as analytical functions. It should be noted that particular forms of f and h are highly dependent on the type of the data, that is these distributions will be different for DSP circuits as compared to random logic modules. This is a point of strength of our approach that enables us to compare the best segmentation architecture for different input data types using analytic or numerical integration techniques as described below.

We first describe a procedure similar to [5] for constructing a segmented channel. We determine a set Λ_k, $0 \leq k \leq K$ such that $0 = \Lambda_0 < \Lambda_1 < \cdots < \Lambda_K = L$. The set of Λ_k's divides the possible net lengths y into a number of ranges $\Lambda_{k-1} < y \leq \Lambda_k$, $k = 1, \cdots, K$. A number of tracks are set aside for nets with lengths in each range (Figure 2a). A group of τ_k identically segmented tracks is placed first, where each track is divided into segments of length Λ_k. Then a second group of τ_k segmented tracks is placed by shifting the previous group of tracks to the right by $\alpha\Lambda_k$ columns for some constant $0 < \alpha \leq 1$ (α is equal to $1/n$ for some positive integer n). The procedure repeats for $1/\alpha$ times. These groups of staggered segmented tracks are placed for every length range to construct a segmented channel.

We adopt this staggered non-uniform segmented channel model with the following assumptions. Let $u = \Lambda_1 \geq 2$ denote the segment length within the set of tracks allocated for net lengths $\Lambda_0 < y \leq \Lambda_1$. The segment lengths for subsequent ranges progress in a **geometric** fashion, i.e., the segment length within the set of tracks allocated for net lengths $\Lambda_{k-1} < y \leq \Lambda_k$ will be u^k. A track which contains segments of length u^k will be referred to as a track of type k. $log_u L$ is an

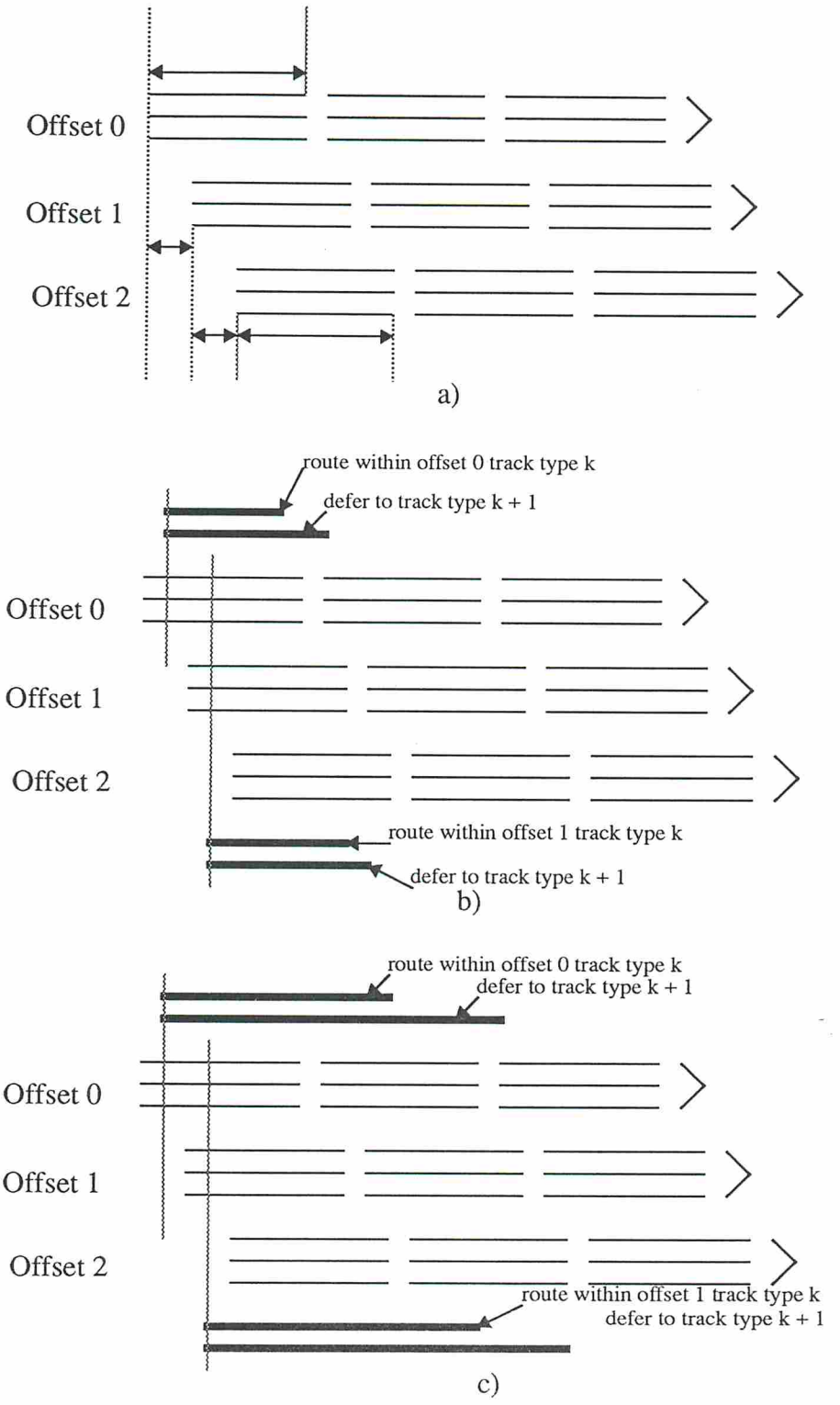

Figure 2: The staggered non-uniform segmentation model (shown for tracks of type k)

integer i.e. the length of the largest segment equals the total length. Short segments are created only at the track boundaries and we will ignore their effects in our analysis.

In the following analysis, we will determine the number τ_k of tracks of type k for $1 \leq k \leq K$ needed for successful routing using one-segmented or two-segmented routing. The total number of tracks T is the sum of τ_k's from 1 to K.

2.2 Routing with One Segment

One-segmented routing is the case when no horizontal fuse is used. This has the advantage of relaxing fuse delay problem. The disadvantage is that when a connection point originates near the end of a segment and spans to a neighboring segment, it cannot be routed by those two segments even if they are the only available ones. On the other hand, two-segmented routing is the case when at most one fuse is used for any connection. The added flexibility in the use of segments makes two-segmented routing more similar to the traditional channel routing.

The following "one-segmented channel routing" scheme is assumed:

Algorithm 2.1

S1: Given the connection length y, select the candidate track of segments u^k, such that $k = \lceil log_u(y) \rceil$;

S2: If routable with one segment then go to S4;

S3: Switch to track of type $k+1$;

S4: Route the connection in the specified track using one segment;

A connection with origination point x and length y is routed either in a segment of length u^k with span $< (j-1)u^k, ju^k >$ such that $(j-1)u^k \leq x < (j-1)u^k + \alpha u^k$ or in one segment of length u^{k+1} with span $< (j-1)u^{k+1}, ju^{k+1} >$ such that $(j-1)u^{k+1} \leq x < (j-1)u^{k+1} + \alpha u^{k+1}$. Therefore, the expected number of tracks of type $k+1$ is the sum of the expected number of tracks used by connections whose length is in the range u^k to u^{k+1} and can be routed in one segment and those whose length is in the range u^{k-1} to u^k and could not be routed using exactly one segment of tracks of type k.

Consider the cases in which *S2* in Algorithm 2.1 succeeds (Figure 2b). Let x and y denote the origination point and the connection length, respectively. Clearly $u^{k-1} < y \leq u^k$. Consider a typical channel segment of type u^k whose leftmost point is at $(j-1)u^k$. The staggered segments of type u^k have their leftmost points at $(j-1)u^k + i\alpha u^k$ for $0 \leq i \leq (1/\alpha - 1)$. In the following cases, the connections with origination point x and length y will be routed using exactly one of these staggered segments.

$$
\begin{array}{ll}
(j-1)u^k < x \le (j-1)u^k + \alpha u^k & u^{k-1} < y \le ju^k - x \\
(j-1)u^k + \alpha u^k < x \le (j-1)u^k + 2\alpha u^k & u^{k-1} < y \le ju^k + \alpha u^k - x \\
\vdots & \vdots \\
(j-1)u^k + i\alpha u^k < x \le (j-1)u^k + (i+1)\alpha u^k & u^{k-1} < y \le ju^k + i\alpha u^k - x \\
\vdots & \vdots \\
ju^k - \alpha u^k < x \le u^k & u^{k-1} < y \le (j+1)u^k - \alpha u^k - x
\end{array}
$$

Thus, the expected number of tracks of type k used by the connections whose length is between u^{k-1} and u^k and originate in the range $(j-1)u^k$ to $(j-1)u^k + \alpha u^k$ is given by:

$$E\{d(j)\} = \int_{(j-1)u^k}^{(j-1)u^k + \alpha u^k} f(x) \int_{u^{k-1}}^{ju^k - x} h(y)dydx$$

However, the number of tracks needed is equal to the maximum density throughout the segmented row. This means, that in order to estimate the number of tracks, one must estimate the expected value of $MAX_j\{d(j)\}$. This is however difficult for arbitrary density functions f and h. We therefore use $MAX_j\{E\{d(j)\}\}$ which is actually a lower bound on $E\{MAX_j\{d(j)\}\}$. Now, the expected number of tracks of type k required to complete the routing of wire connections whose length is between u^{k-1} and u^k and originate in the range $(j-1)u^k$ to $(j-1)u^k + \alpha u^k$ for $1 \le j \le L/u_k$ is given by:

$$MAX_{j=1}^{L/u^k} E\{d(j)\}$$

and the expected number of staggered tracks of type k required to complete the routing of wire connections whose length is between u^{k-1} and u^k is given by:

$$n_1^k = \sum_{i=0}^{1/\alpha - 1} MAX_{j=1}^{L/u^k} \int_{(j-1)u^k + i\alpha u^k}^{(j-1)u^k + (i+1)\alpha u^k} f(x) \int_{u^{k-1}}^{ju^k + i\alpha u^k - x} h(y)dydx$$

Next consider cases in which *S2* in Algorithm 2.1 fails (Figure 2b). Note that these connections will be "deferred" to next larger track type and will be successfully routed there (without any further deferrals).

$$
\begin{array}{ll}
(j-1)u^k < x \le (j-1)u^k + \alpha u^k & ju^k - x < y \le u^k \\
(j-1)u^k + \alpha u^k < x \le (j-1)u^k + 2\alpha u^k & ju^k + \alpha u^k - x < y \le u^k \\
\vdots & \vdots \\
(j-1)u^k + i\alpha u^k < x \le (j-1)u^k + (i+1)\alpha u^k & ju^k + i\alpha u^k - x < y \le u^k \\
\vdots & \vdots \\
ju^k - \alpha u^k < x \le ju^k & (j+1)u^k - \alpha u^k - x < y \le u^k
\end{array}
$$

Thus, the expected number of tracks of type $k+1$ used by the connections whose length is between u^{k-1} and u^k and originate in the range $(j-1)u^k$ to $(j-1)u^k + \alpha u^k$ is given by:

$$E\{d'_j\} = \int_{(j-1)u^k}^{(j-1)u^k + \alpha u^k} f(x) \int_{ju^k - x}^{u^k} h(y)dydx$$

The expected number of staggered tracks of type $k+1$ required to complete the routing of wire connections whose length is between u^{k-1} and u^k is given by:

$$m_1^k = \sum_{i=0}^{1/\alpha-1} MAX_{j=0}^{L/u^k} \int_{(j-1)u^k+i\alpha u^k}^{(j-1)u^k+(i+1)\alpha u^k} f(x) \int_{ju^k+i\alpha u^k-x}^{u^k} h(y)dydx$$

Finally, the expected number of staggered tracks of type k required to complete the routing of wire connections that are assigned to these tracks by the one-segmented channel router is:

$$\tau_1^k = n_1^k + m_1^{k-1}$$

where n_1^k denotes the expected value of the number of necessary tracks to route successfully connections whose length are between u^{k-1} and u^k and m_1^{k-1} denotes the expected value of required number of tracks to route such connections of length u^{k-2} and u^{k-1} which cannot be routed using tracks of type $k-1$.

2.3 Routing with Two Segments

The following "two-segmented channel routing" scheme is assumed.

Algorithm 2.2

S1: Given the connection length y, select the candidate track of type k where $k = \lceil log_u(y) \rceil - 1$;

S2: If routable with two segments then go to S4;

S3: Switch to track of type $k+1$;

S4: Route the connection in the specified track using one or two segments;

Clearly, $u^k < y \leq u^{k+1}$. Cases in which S2 in Algorithm 2.2 succeeds are the following (Figure 2c).

$(j-1)u^k < x \leq (j-1)u^k + \alpha u^k$	$u^k < y \leq (j+1)u^k - x$
$(j-1)u^k + \alpha u^k < x \leq (j-1)u^k + (i+1)\alpha u^k$	$u^k < y \leq (j+1)u^k + \alpha u^k - x$
$\vdots$	$\vdots$
$(j-1)u^k + i\alpha u^k < x \leq (j-1)u^k + (i+1)\alpha u^k$	$u^k < y \leq (j+1)u^k + i\alpha u^k - x$
$\vdots$	$\vdots$
$ju^k - \alpha u^k < x \leq ju^k$	$u^k < y \leq (j+2)u^k - \alpha u^k - x$

Omitting details, we obtain:

$$n_2^k = \sum_{i=0}^{1/\alpha-1} MAX_{j=1}^{L/u^k} \int_{(j-1)u^k+i\alpha u^k}^{(j-1)u^k+(i+1)\alpha u^k} f(x) \int_{u^k}^{(j+1)u^k+i\alpha u^k-x} h(y)dydx$$

Cases in which S2 in Algorithm 2.2 fails are the following (Figure 2c). Note that these connections will be deferred to next larger track type and because of the two-segmented routing scheme will be successfully routed there (without any further deferrals).

$$
\begin{array}{ll}
(j-1)u^k < x \leq (j-1)u^k + \alpha u^k & (j+1)u^k < y \leq u^{k+1} \\
(j-1)u^k + \alpha u^k < x \leq (j-1)u^k + (i+1)\alpha u^k & (j+1)u^k + \alpha u^k - x < y \leq u^{k+1} \\
\vdots & \vdots \\
(j-1)u^k + i\alpha u^k < x \leq (j-1)u^k + (i+1)\alpha u^k & (j+1)u^k + i\alpha u^k - x < y \leq u^{k+1} \\
\vdots & \vdots \\
ju^k - \alpha u^k < x \leq ju^k & (j+2)u^k - \alpha u^k - x < y \leq u^{k+1}
\end{array}
$$

Omitting details, we obtain:

$$m_2^k = \sum_{i=0}^{1/\alpha - 1} MAX_{j=1}^{L/u^k} \int_{(j-1)u^k + i\alpha u^k}^{(j-1)u^k + (i+1)\alpha u^k} f(x) \int_{(j+1)u^k + i\alpha u^k - x}^{u^{k+1}} h(y) dy dx$$

Finally, the expected number of tracks of type k required to complete the routing of wire connections that are assigned to these tracks by the two-segmented channel router is:

$$\tau_2^k = n_2^k + m_2^{k-1}$$

where m_2^{k-1} is the contribution of connections of length u^{k-1} and u^k and n_2^k is the contribution of connections of length u^k and u^{k+1}.

2.4 Remarks

We therefore showed how to obtain the track type distributions τ_1^k and τ_2^k under the one-segmented and two-segmented routing models. This information is used to calculate the required number of tracks of type k subject to given number of tracks in the routing channel. Our derivations are general and independent of the particular forms of distributions of f (origination point) and h (connection length). Once these distributions are known, the optimal staggered non-uniform channel architecture can be generated.

3 Study of Architectures for Specific Distributions

In this section, we give closed form expressions for two interesting and commonly used special cases. We have used continuous density functions, in the case of discrete density functions which are represented by histograms, a curve fitting technique can be used to produce the continuous functions and then closed form expressions can be derived. Alternatively numerical integration techniques may be applied. The staggered non-uniform segmented channel model already fixes the architecture to a great extent. The free parameters of the architecture are u, α, and τ^k. We show how to apply the derivations in section 2 to some prevalent distributions. We have picked two example distributions. Similar calculations could be done for other types of distributions. In both

cases we assume that the origination point has *uniform* distribution. This choice of distribution for the origination point is very close to reality as confirmed by empirical studies by the authors as well as the others.[9]

3.1 Uniform Connection Length

If we assume that both the connection length and origination point have *uniform* distributions, n_1^k and m_1^k can be expressed in closed forms. The choice of uniform distribution for the connection length corresponds to a random placement of of modules on the FPGA device. We are presenting this case only for the sake of illustration. Uniform distribution implies that $f(x) = N/L$ and $h(x) = 1/L$ where N denotes the total number of connections. Thus,

$$n_1^k = \frac{Nu^{2k}}{L^2}(1 - \frac{\alpha}{2} - \frac{1}{u})$$

$$m_1^k = \frac{Nu^{2k}}{L^2}\frac{\alpha}{2}$$

$$n_2^k = \frac{Nu^{2k}}{L^2}(1 - \frac{\alpha}{2})$$

$$m_2^k = \frac{Nu^{2k}}{L^2}(-2 + \frac{\alpha}{2} + u)$$

These formulas indicate an exponential increase in the number of required tracks as k increases. This makes sense if we recall that the uniform connection length suggests that the number of short and long connections are equal, and that the segment lengths on FPGA tracks with short and long segments differ in an exponential fashion. Thus, exponentially more tracks with long segments are required to accommodate the same number of connections.

3.2 Exponential Connection Length

Another interesting case is when the origination point is uniform, but the connection length has an exponential distribution, that is, $f(x) = N/L$ and $h(x) = \lambda e^{-\lambda x}$. λ is the inverse of the expected value of connection length. This corresponds to the wire length distribution after placement optimization. Keeping in mind that exponential distribution is the continuous counter part of geometric distribution, it seems to fit better to empirical data and our results confirm it. The relevant closed form expressions are as follows:

$$n_1^k = \frac{N}{L}\left(u^k e^{-\lambda u^{k-1}} - \frac{1}{\alpha\lambda}(e^{-(1-\alpha)\lambda u^k} - e^{-\lambda u^k})\right)$$

$$m_1^k = \frac{N}{L}\left(\frac{1}{\alpha\lambda}(e^{-(1-\alpha)\lambda u^k} - e^{-\lambda u^k}) - u^k e^{-\lambda u^k}\right)$$

$$n_2^k = \frac{N}{L}\left(u^k e^{-\lambda u^k} - \frac{1}{\alpha\lambda}(e^{-(2-\alpha)\lambda u^k} - e^{-2\lambda u^k})\right)$$

$$m_2^k = \frac{N}{L}\left(\frac{1}{\alpha\lambda}(e^{-(2-\alpha)\lambda u^k} - e^{-2\lambda u^k}) - u^k e^{-\lambda u^{k+1}}\right)$$

4 Example of Architecture Evaluation

Now we have a tool at our disposal to evaluate the effectiveness of candidate segmented channel architectures. We show that when an archiecture is already given, there is a measure which can be used to predict its success rate, i.e. the percentage of connections that can be successfully routed. The formula presented hereafter compares the results of estimations for required number of tracks with the actual architecture.

Let a_k denote the number of tracks of type k in a given segmented channel architecture and τ_k denote the expected number of tracks of type k calculated in section 2 for one- (or two-segment routing schemes whatever the case maybe). In general, f and h are different for control-dominated versus data-path dominated designs, thus, τ_k's calculated for these classes of designs will be different.

Consider choosing between two channel segmentation architectures for a new class of circuits with its specific f and h. The following analysis will determine which of the two architectures is more suitable. We exemplify the problem with arbitrary data, though it can be extracted from real architecture.

We define a function called $surplus(k)$ as follows:

$$surplus(0) = 0;$$

$$surplus(k) = (\tau_k - a_k + surplus(k-1))S(\tau_k - a_k + surplus(k-1));$$

where $S(x)$ is the unit step function.

Since K denotes the largest available track type, $surplus(K)$ gives the number of tracks that cannot be routed. We conclude that the percentage of unsuccessful routing is:

$$\frac{surplus(l)}{\sum_{k=1}^{l} \tau_k}$$

ARCHITECTURE 1.

a_k	τ_k	$surplus(k)$
7	10	10-7+0=3
8	10	10-8+3=5
18	10	0
9	10	10-9+0=1
8	10	10-8+1=3

that is, %6 of the connections cannot be successfully routed.

ARCHITECTURE 2.

a_k	τ_k	$surplus(k)$
12	10	0
9	10	10-9+0=1
8	10	10-8+1=3
11	10	10-11+3=2
10	10	10+2-10=2

that is, %4 of the connections cannot be successfully routed. We therefore conclude that the second segmented architecture is superior for the given design data.

5 Empirical Results

A program in C was developed to compute our estimations and generate the channel architecture. Short segments were generated only at the boundaries of the segmented track. The algorithms for one-segmented and two-segmented routing are from Zhu et al. [12]. Tables 2 and 3 show our results. u is the ratio of length of segments of tacks of type $k+1$ and k. α is the offset ratio. λ is the parameter of the exponential distribution. NT is the total number of tracks in the routing channel. We generate 100 random routing problems. The success rate denotes the percentage of problems which were successfully routed on the specified architecture using the fixed number of tracks. Threshold Density d_T, is defined as the smallest channel density d such that less than %90 of the channels with density d in the distribution are successfully routed with segmentation. The fixed parameters of the routing channel are given in table 1.

Maximum number of nets per channel	121
Minimum number of nets per channel	31
Maximum net length	99
Minimum net length	1
Maximum channel density	36
Number of columns	100
Number of channels generated	100
Number of connections	68

Table 1: Parameters for the random channels

As we predicted the percentage of successful routing is highly dependent on the type of the distributions and their parameters. Based on the maximum channel density restriction, we scaled our estimations up or down linearly. The length of the longest segment was taken to be the channel length and no offset was considered for the last track. Up to %83 of channels generated according to our model were successfully routed when the exponential distribution model and two segment routing algorithm were used. The best result obtained when one segment routing were used was %73 successful routing completion. Our results compare very favorably to those reported by Zhu et al. [12] and Greene et al. [6].

In the case of exponential distribution model, the best results are obtained when the expected value of the length is between 1/5 to 1/3 of the channel length.

6 Concluding Remarks

We addressed the channel segmentation design and the routability analysis for row-based FPGA devices. Our formulation is quite general and can handle arbitrary density functions for the origination point and length of connections. At the same time, it captures the essential features of the segmented routing scheme that is to be used. We relied on the staggered non-uniform segmentation model for our analysis and derived expressions for the desired number of tracks of each type. Although we derived expressions for one- and two-segmented routing only, generalization to M-segmented routing is straight-forward.

Architecture				Results	
u	α	λ	NT	Success Rate	Threshold Density
4	0.25	0.06	38	%72	28
4	0.25	0.055	39	%73	28
3	0.33	0.06	39	%66	26
3	0.33	0.0525	39	%68	24
3	0.33	0.05	38	%65	24

Table 2: Results after implementing one segment routing. All the above results were generated when the exponential length formulas for one segment routing were applied and exponentially distributed random channels were used. The legends are as follows: 'NT' is total number of tracks generated. 'Success Rate' is the percentage of successfully routed channels. 'Threshold Density' d_T, is defined as the smallest channel density d such that less than %90 of the channels with density d in the distribution are successfully routed with segmentation.

Architecture				Results	
u	α	λ	NT	success rate	Threshold Density
4	0.25	0.05	37	%80	25
4	0.25	0.045	37	%77	26
4	0.25	0.033	37	%72	28
3	0.33	0.05	38	%83	31
3	0.33	0.045	39	%83	29
3	0.33	0.033	39	%82	29
2	0.5	0.06	39	%77	26
2	0.5	0.055	39	%79	26
2	0.5	0.04	38	%80	29

Table 3: Results after implementing two segment routing. All the above results were generated when the exponential length formulas for two segment routing were applied and exponentially distributed random channel were used.

The main benchmark of our calculations is that given the corresponding data histograms, for any application we can predict the number of necessary tracks. Our calculations facilitate the evaluation of the different architectures and find the one that has the highest probability of routing completion.

We are currently looking into relaxing other fixed features of the segmentation model, that is, varying offsets, non-geometric segment length progression, non-uniform segment length within the same track, etc. This will allow us to use more realistic segmentation model for the two- and M-segmented routing. We intend to model more sophisticated routing schemes (such as those presented by [2, 12]) and derive expressions that describe their performance on a given segmentation architecture.

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