Variations in Electrical Values and their Ramifications on Correct Circuit Operation

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CENG 97-06

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January 1997

Variations in Electrical Values and their Ramifications on Correct Circuit Operation [1]

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Abstract

Modern designs employ deep sub-micron technology and high clock frequencies. These factors require designers to pay close attention to the electrical properties of circuits in order to control the effects of factors such as crosstalk, ground bounce, signal reflection and clock skew. Because of normal process variations in the fabrication of VLSI chips, electrical parameters vary. In this paper, two areas are addressed. The first deals with measuring the variations in the values of the electrical parameters such as resistance and capacitance, found in good (fault-free) die. In addition correlations between these variations were determined. For example we found that the area capacitance between Metal2 and PWELL substrate varied by as much as 55% and that the gain factors of P and N channel transistors were highly correlated. In the second part of this paper, we discuss the results of some simulation studies carried out to determine the magnitude of the effect of the variations in the value of electrical parameters on (1) simple signal propagation delay, (2) delay due to crosstalk, and (3) the magnitude of crosstalk pulse. We found large variations in the delay values and in the voltage of the pulse. From these results one can identify new design corners that should be considered during design, and other design corners that can be ignored.

1 Introduction

In modern digital designs employing high clock frequencies and low feature sizes, factors such as electromagnetic interference between signal lines assume more significance. These factors may lead to erroneous circuit operation due to such effects as crosstalk ([4], [5], [6] and [1]) and ground bounce ([2]). To determine the extent of such interferences, the precision with which the various electrical parameters, such as resistance and capacitance, can be controlled in a process has to be evaluated. Once the precision is known, then process corners can be identified. The importance of developing new validation strategies due to the presence of such process aggravated noise (PAN) has been stressed in [3]. In this project we estimate the precision of a 0.8 micron process by computing the variations in electrical parameters, such as resistance, of different features, such as transistors and wires, in a process run spanning about one year. The variations thus obtained are then used to demonstrate the impact of process variations on circuit operations such as signal delay and crosstalk effects via simulation of example circuits. The variations in the values of passive parameters such as capacitances are not currently considered during the validation of digital circuits [8]. Such parametric variations and their strong influence on circuit performance

[1]This work was supported by the Advanced Research Projects Agency and monitored by the Department of the Army, Ft.Huachuca, under Contract No. DABT63-95-C-0042. The information reported here does not necessarily reflect the position or the policy of the Government and no official endorsement should be inferred.

are brought to light. The importance of correlations between parameters in identifying realistic design corners is also emphasized.

This project was carried out with the cooperation of the Information Sciences Institute (ISI) of the University of Southern California. ISI runs the MOSIS service which provides a brokering service for manufacturing low volume custom VLSI chips for customers such as academic institutions. The wafers provided to customers of MOSIS are fabricated by major IC manufacturers as part of their normal daily runs. The statistical inferences in this paper are based on the data set ([7]) provided to us by ISI.

The process which we are analyzing is a 0.8 micron process with a single poly layer, three metal layers, and uses 13 masks. The poly and diffusion are silicided. The process uses LDD technology.

The paper is organized as follows. Sections 2, 3, 4 and 5 provide the goal, a detailed account of the parameters of interest, their measurement, organization and computation. Sections 6 and 7 deal with the types of analysis performed on the data and the results and statistical inferences obtained. The impact of these results are elucidated through three examples discussed in Section 8. Section 9 gives our conclusion.

2 Goals

The goal of this project is to estimate the variations in the values of electrical parameters, such as Metal1-Metal2 capacitance and metal sheet resistance, due to normal process variations, and to demonstrate the impact of such variations on the performance of VLSI circuits. Further, it is aimed to incorporate the information on these parameter variations into design and validation methodologies and to utilize this information to identify realistic design corners for the aggressive design of high speed deep submicron circuits.

3 Electrical Parameters

Process data obtained from the MOSIS service was used to estimate the variations in electrical parameters. A brief description of the MOSIS Process Monitor (PM), the parameters of interest that are being measured, the test structures employed for estimating the parameter values and the computation of the parameters are given in the following subsections ([7]).

3.1 The MOSIS Process Monitor

The MOSIS Process Monitor (PM) consists of an array of AC and DC parametric test structures and a small number of functional test devices for monitoring the fabrication of wafers for the MOSIS service. These tests are designed to monitor all of the parameters that are in the vendor process specification for each supported technology.

There are three classes of test devices: DC parametric, AC parametric, and functional. Each class of test device has its own group of probe card pins. The DC parametric area consists of a 2×10 pad group that is tested entirely by instrumentation within a parametric tester. The AC parametric area (capacitors) consists of a 2×3 pad group wired directly, through isolation relays,

to a HP 4275A LCR meter which is interfaced to the Parametric Tester through a IEEE-488 bus. The functional device test area consists of a 2×10 pad group that is interfaced to an IMS functional test system and HP frequency counter. Both are also interfaced to the parametric tester through a IEEE-488 bus.

3.2 Electrical Parameters

Good wafers are selected based on whether certain measured electrical parameter values are within specified values. The following electrical parameters are of interest to us:

- Interconnect Parameters
  1. Contact Resistance
  2. Sheet Resistance
  3. Line Width
- Transistor Characteristics
  1. Voltage Threshold (for P and N channel)
  2. Process Gain Factor
- Capacitors
  1. Area Capacitance
  2. Fringe Capacitance

The test structures used for the measurement of raw data used for the computation of the above parameters are given next.

3.3 Test Structures

3.3.1 Interconnect Parameters

Contact Resistance: This parameter is measured using bridges which are Kelvin-connected contact resistors with a single contact between two connected layers on the chip. The test structure is shown in Figure 1. Two variations of contact resistors are available: one with a large overlap around the contact and another with a minimum overlap allowed by the design rules.

Testing is performed by passing constant current (I_{force}) through the contact between the two layers and measuring the resulting voltage. The contact resistance is given by $R_c = V_{measure}/I_{force}$ Ohms, where $V_{measure}$ is the measured voltage and I_{force} is 1.0mA for cuts and 10.0mA for vias.

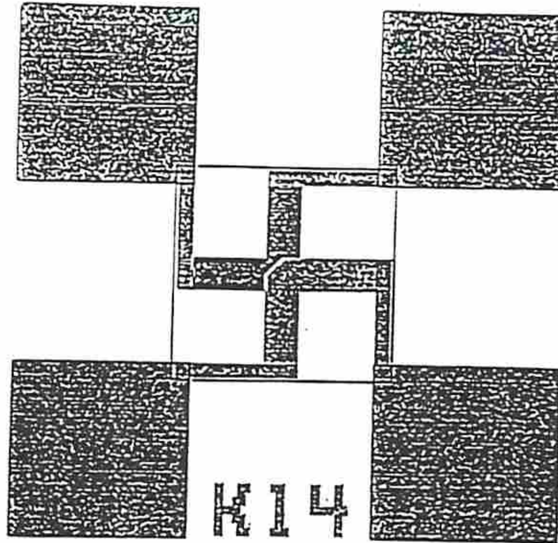


Figure 1: Test Structure for Contact Resistance

Sheet Resistance and Line Width: These parameters are measured using a test structure called a Split bridge. The test structure is shown in Figure 2. This split bridge consists of a Van der Pauw crossed bridge for sheet resistance measurement, a Kelvin line width measurement section, and a split wire section. The Van der Pauw section is a classic four arm structure. Testing consists of a Van der Pauw measurement which involves passing current (I_{force}) through two adjacent arms of the crossed bridge and measuring voltage on diagonal pair of arms. The measurement is repeated with the pairs of arms for current force and for voltage sense rotated 90 degrees on the crossed bridge. Wire width measurements are taken by passing constant current through the entire length of the structure and measuring the voltage between taps on the wire.

The two voltage readings are averaged to remove any possible asymmetry in the bridge. The sheet resistance is given by $R_s = (\pi/ln2) * (AV_{measure}/I_{force})$ Ohms/square where $AV_{measure}$ is the averaged voltage, and I_{force} is 75mA for Metal2, 40mA for Metal1, 1.0mA for Active regions and Poly and 10.0μA for Well.

The line width is given by $W_{eff} = (R_s \times L)/(V_B/I_{force})\mu$m where V_B is the measured bridge tap voltage, L is the designed wire bridge tap spacing (120 μm) and I_{force} is the test current and is 40mA for Metal2, 15mA for Metal1, 0.1mA for Active regions and Poly and 1.0uA for Well.

3.3.2 Transistor Characteristics

Voltage Threshold: The threshold voltages are obtained from a conductivity curve which is a plot of drain current versus gate voltage for a drain voltage that is much less than twice the Fermi potential ($2 * \phi$). The absolute drain voltage is set at 50mV. The threshold voltage is found by extrapolating the linear portion of the conductivity curve to $I_d = 0$.

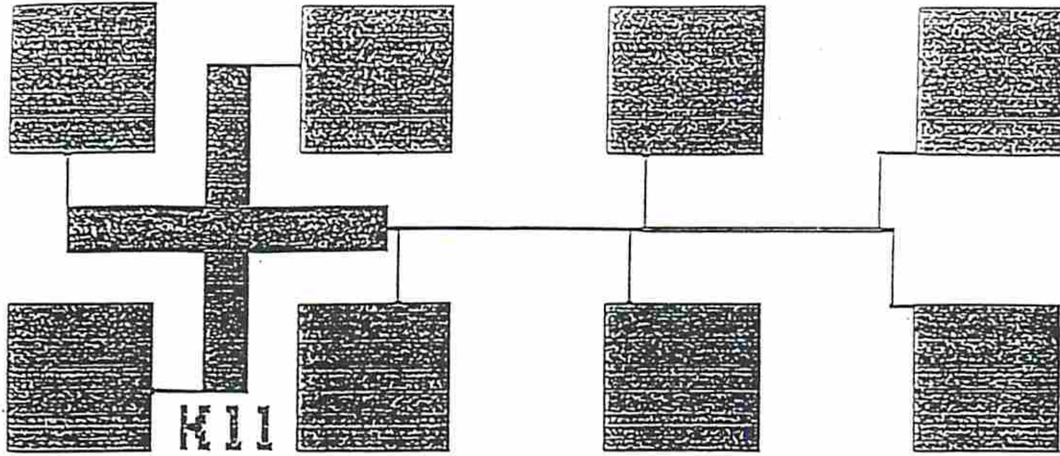


Figure 2: Test Structure for Sheet Resistance

Process Gain Factor: The slope of the conduction curve obtained in the threshold voltage measurement process is used to calculate the process gain factor. The slope of the conduction curve is $2 * K * V_d$. Hence $K = S/(2 * V_d)$. Since $K = K' * (W/L)$, where K' is the process gain factor, K' is calculated from $K' = (S/(2V_d)) * (L/W)$. Here W and L are corrected for as-fabricated W and L to give effective channel width and length. The effective channel length and width are given by $L = L_drawn - DL$ and $W = W_drawn - DW$, where $DL = (L1 * S1 - L2 * S2)/(S1 - S2)$ for transistors with $W1 = W2$, and $DW = (W1 * S2 - W2 * S1)/(S2 - S1)$ for transistors with $L1 = L2$.

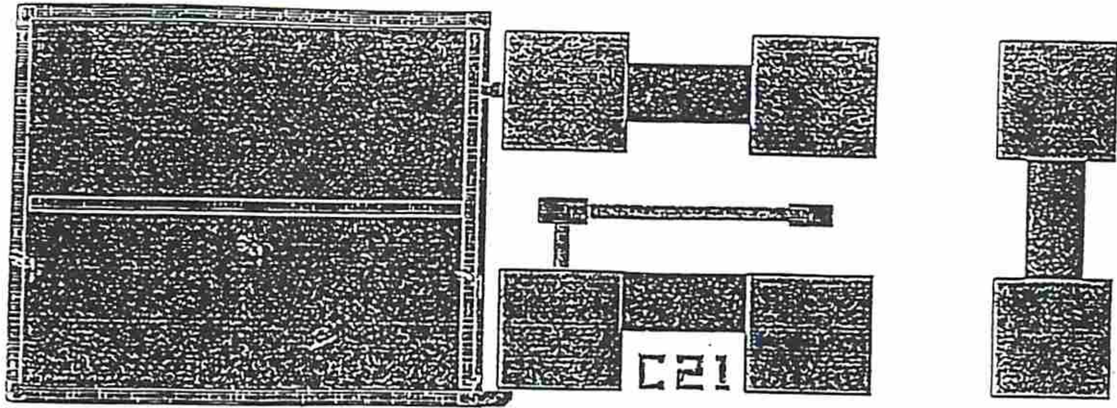
3.3.3 Capacitance Parameters

Area Capacitors: The area capacitors are designed with the top electrode dimensions set at 240 μm high by 300 μm wide. The test structure is shown in Figure 3.

Measurements are made with an AC test voltage of 100 mV rms and a frequency of 100 KHz. The measurement gives the area capacitance as C_{am}. The unit area capacitance is obtained by dividing C_{am} by the area of the capacitor, A_a, which is $72000 \mu m^2$.

Fringe Capacitors: The fringe capacitors are comb structures with a comb width of 10 μm and a comb spacing of 10 μm. The height is slightly smaller than 240 μm, the maximum height permitted by the capacitor structures. The top electrode length is 300 μm. The test structure is shown in Figure 4.

Measurements are made with an AC test voltage of 100 mv rms and a frequency of 100 KHz. The measurement gives the fringe capacitance as C_{fm}. The capacitance per unit length is



Area Capacitor POLY to P_PLUS_ACTIVE

Figure 3: Test Structure for Area Capacitance

obtained by dividing C_{fm} by the perimeter of the fringe capacitor, P_f, which is 7500μm.

Calibration Capacitors: There are two six-pad calibration capacitors provided to measure and store the stray capacitance associated with the test fixture for deduction from subsequent measurements. One calibration capacitor is floating so it can be used to calibrate out stray capacitances involved in measuring capacitors that do not have one electrode connected to the substrate, e.g., a Metal1 to Metal2 capacitor. The other calibration capacitor has one electrode connected to the substrate to calibrate out stray capacitances that are seen when measuring capacitors that use the substrate as one electrode, e.g., Metal2 to substrate.

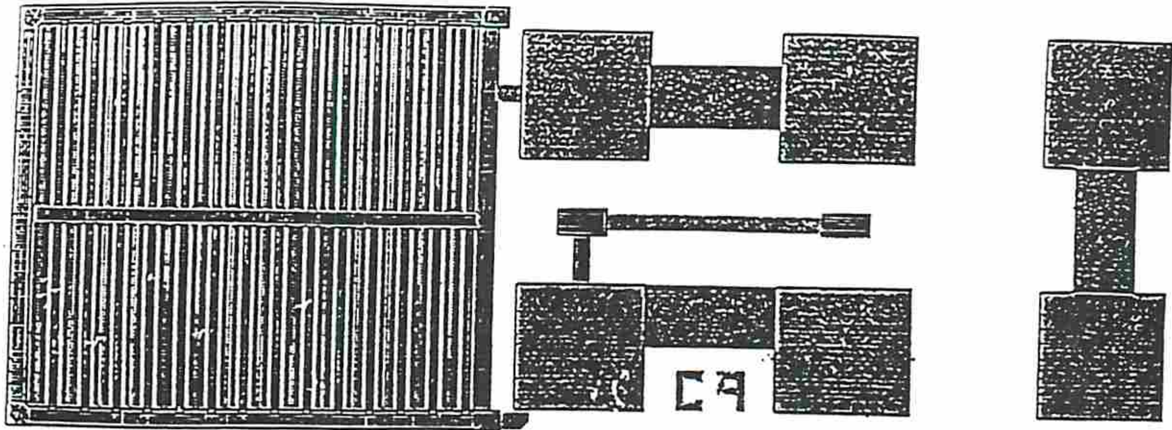
Component Capacitances: Computation of component capacitances, e.g., junction capacitance CJSW and CJ, using the area capacitor measurements and the fringe capacitor measurements is done with the following equations.

- Fringe Capacitance

$$C_f = ((C_{am}/A_a) - (C_{fm}/A_f))/((P_a/A_a) - (P_f/A_f))pF/\mu\text{m}$$

- Area Capacitance

$$C_a = (C_{am}/A_a) - C_f * (P_a/A_a)pF/\mu m^2$$



Fringe Capacitor P_PLUS_ACTIVE to N_WELL

Figure 4: Test Structure for Fringe Capacitance

where C_{am} and C_{fm} are the measured area capacitance and fringe capacitance respectively; A_a and A_f are the area of the area capacitor and fringe capacitor respectively; and P_a and P_f are the perimeters of the area capacitor and fringe capacitor, respectively.

4 Volume and Structure of Data

The work reported here is based on measurement, made on a set of 15 wafer lots. Each wafer lot has a certain number of wafers ranging from 3 to 10. There are a total of 66 wafers in this population. Each die on the wafer has a complete set of test structures for each parameter (such as voltage threshold of a transistor). However, measurements are made on only 9 dies on each wafer. These 9 locations are the same for each wafer in a lot, but may vary over lots. Hence, we have 9 x 66 = 594 points of measurement in total for any given parameter. As mentioned before, some electrical parameters were directly obtained by measurement while others had to be computed using a formula and measured data values.

For transistors, there are 32 voltage threshold measurements per die and 32 gain factor computations per die. The 32 measurements are for different sizes of the transistors under different bulk to substrate bias conditions. Sheet resistances are given for 6 layers on each die. Line widths are also given for the 6 layers. Contact resistances are given for 8 different contacts on a die. There are 14 area capacitance measurements and 4 fringe capacitance measurements. The list of parameters measured is given in Appendix I. It should be noted that only values associated with good wafers are used in this study. All the values lie between the upper and lower bounds as guaranteed by the manufacturer. Wafers that were suspected of being bad have

been discarded.

5 Computation of Parameters

The electrical parameters of interest are obtained either directly by measurement or through computation. The voltage threshold and contact resistance are obtained directly from the data files. Gain factor, sheet resistance, area capacitances and fringe capacitances have to be computed. The formulae used for the computations have been given in section 3.3. However, certain approximations to the formulae have been made for statistical reasons. Also, some data values that are extremely far from the nominal expected value and assumed to be in error are ignored. These data values are referred to as outliers.

The gain factor calculation ignores DL and DW. This is because the computation of these involve the use of the slopes of the gain factor curves (the measured S values) of other transistors on the die. Hence, a wide variation in them or even the presence of outliers would affect the computation of the DL and DW values leading to a distorted picture of the variations of the gain factors. The drawn values of the channel length and width were used to compute the gain factor using the formulae given in section 3.3.2.

In the computation of component area capacitances (CJ) the fringe effect (term involving C_f) was ignored since the fringe measurements were found to be unreliable. Moreover, the fringe factor is actually less than 1% of the area capacitance per unit area. Hence the component area capacitance becomes $C_a = C_{am}/A_a$.

6 Types of Analysis

Different types of analysis were performed to draw inferences on the statistical nature of the data.

6.1 Histograms

For each parameter, the data set comprises of 594 points in total. A histogram was obtained to observe the distribution of the data points. The x-axis of the histogram was normalized to percentage deviation from the mean. Moreover, statistics consisting of the mean, the standard deviation as a percentage of the mean, and the worst case deviation (max - min) as a percentage of the mean were also computed.

Analysis was also done on the largest wafer lot. Histograms and allied statistics were obtained for three cases:

- Case 1: for the entire wafer lot
- Case 2: for each data point having the same coordinate over all the wafers in the wafer lot, for all nine coordinates
- Case 3: for all nine data points on each wafer over all the coordinates and for all wafers in the wafer lot.

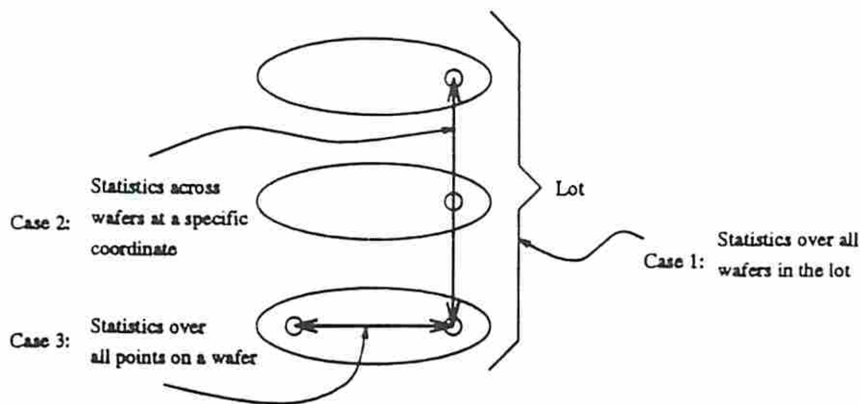


Figure 5: Analysis on the largest wafer lot

Figure 5 illustrates the types of analysis done on the largest wafer lot as listed above.

A typical histogram that was generated is shown in Figure 6. This histogram corresponds to the sheet resistance of Metal1 as indicated by the acronym SR.

6.2 Sequence Plots

The wafers within a lot are assumed to be manufactured at the same time. Hence, there is no chronological ordering among wafers within a lot. A sequence plot consists of data values within each lot ordered in ascending order by value and the lots are ordered by the time they were manufactured.

The sequence plot was obtained to identify any change points in the data and to locate anomalies in the data set.

A typical sequence plot is shown in Figure 7. This sequence plot corresponds to the sheet resistance of Metal1. The exhaustive list of parameters and their acronyms as they appear on the graphs are given in Appendix I. Sample plots of either type are provided in Appendix II.

6.3 Correlation Coefficients

This is a statistic estimated for each pair of parameters to identify any correlation between them. The correlation coefficient C of two parameters represented by random variables X and Y is given by

$$C = covariance(X, Y)/(stdev(X) * stdev(Y))$$

The extreme values for this coefficient are +1 and -1. +1 signifies that the X and Y variations are in the same direction and -1 signifies that the X and Y variations are in the opposite direction. Intermediate values signify varying degrees of correlation. A value of 0 indicates no correlation i.e. X and Y are independent.

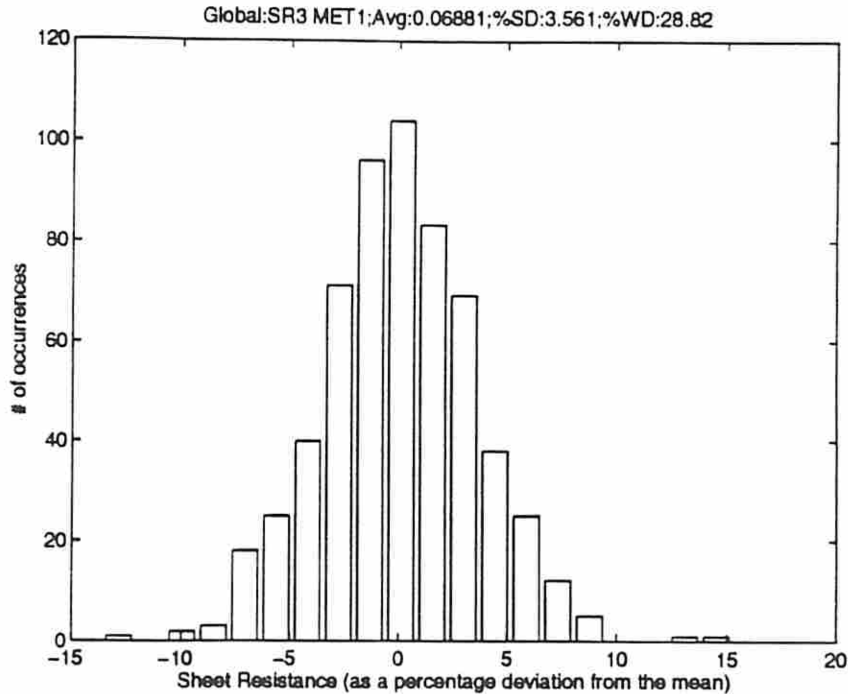


Figure 6: Histogram of Metal1 Sheet Resistance Values

7 Results and Inferences

The results and inferences of the analysis are presented below. The individual parameter variations are given first followed by the correlation results.

7.1 Individual Parameter Variation Results

The individual parameter variations were estimated over the global population as well as for the largest wafer lot.

7.1.1 Global Variations

The variations of parameters over the entire population is presented in Table 1. The first three columns show the mean, standard deviation as a percentage of the mean, the worst case deviation (maximum value - minimum value) as a percentage of the mean respectively. If the distributions of the parameter values were normal, then it can be assumed that mean plus thrice the standard deviation would cover 99.7% of the points. However, the distributions are not exactly normal. Hence, the percentage deviation from the mean required on either side of it to cover 98%, 96% and 95% of the data points in the respective distributions are calculated and tabulated in the last three columns of Table 1.

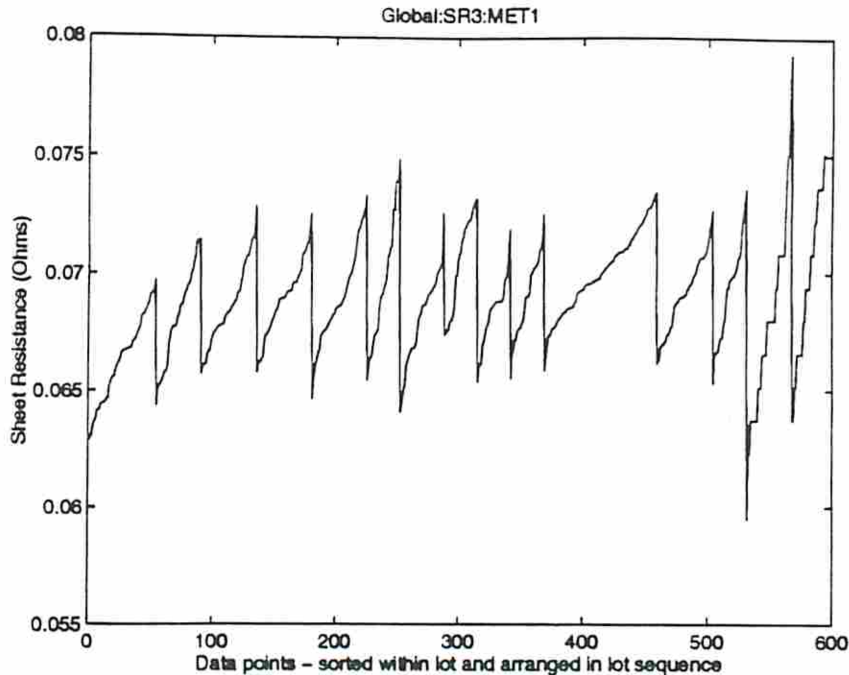


Figure 7: Sequence plot of Metal1 sheet resistance values

7.1.2 Largest Lot Variations

The variations within the largest wafer lot along with the variations in the global population is presented in Table 2 for comparison.

7.2 Inferences on Individual Parameter Variations

The amount of variation in the different parameters follow the order shown below:

Fringe capacitance > Contact resistance > Area capacitance > Sheet resistance > Gain factor > Voltage threshold

7.2.1 Global Inferences

The following individual inferences are based on trends in the standard deviations of the individual parameters.

- Voltage Threshold: No remarkable change in the variation statistics was observed with change in the size of the transistor for a particular bias condition.
- Contact Resistance: The deviations are in the following order:

  Metal2 - Metal3 > Metal1 - Metal2 > P+ - Metal1, N+ - Metal1, Poly - Metal1

  This ordering may be due to the nature of the specific process being employed.

Electrical Parameters		Mean Value	% Standard Deviation	% Worst Case Deviation	% Deviation from Mean covering x% of the points		
					x = 98%	x = 96%	x = 95%
Voltage Threshold	N:1.2/0.8	0.76 V	2.76%	15.7%	6.29%	5.76%	5.23%
	P:1.2/0.8	-0.91 V	2.35%	14.2%	5.21%	4.74%	4.26%
Gain Factor	N:1.2/0.8	$3.73 \times 10^{-5} A/V^2$	7.48%	38.8%	15.51%	14.21%	14.2%
	P:1.2/0.8	$9.04 \times 10^{-6} A/V^2$	6.67%	31.4%	12.54%	12.54%	11.49%
Sheet Resistance	P+ Diff	2.05 Ohms	6.41%	31.6%	13.69%	12.64%	12.63%
	Poly	2.08 Ohms	6.60%	46.3%	16.99%	13.9%	13.9%
	Metal1	0.07 Ohms	3.56%	28.8%	8.64%	7.68%	6.72%
	Metal2	0.07 Ohms	2.98%	19.9%	6.66%	5.99%	5.99%
Line Width	Metal1	3.76 μm	5.26%	29.3%	10.75%	8.79%	8.79%
	Metal2	3.61 μm	5.21%	20.1%	9.38%	8.71%	8.04%
Contact Resistance	P+ Diff - Metal1	1.23 Ohms	4.24%	26.4%	10.56%	8.80%	7.92%
	Metal1 - Metal2	0.49 Ohms	19.23%	116.0%	50.27%	38.67%	34.80%
Area Capacitance	Metal2 - Metal3	$3.2 \times 10^{-17} F/\mu m^2$	9.24%	41.9%	19.55%	18.15%	16.76%
	Poly - Metal2	$2.27 \times 10^{-17} F/\mu m^2$	6.34%	26.9%	12.55%	11.66%	11.66%
	Metal1 - Metal2	$3.03 \times 10^{-17} F/\mu m^2$	5.75%	30.0%	13.0%	12.0%	11.0%
	Metal1 - PWELL	$4.37 \times 10^{-17} F/\mu m^2$	6.46%	36.5%	24.34%	21.90%	8.52%
	Metal2 - PWELL	$2.34 \times 10^{-17} F/\mu m^2$	11.03%	55.2%	29.46%	25.78%	18.41%
Fringe Capacitance	P+ Diff - Poly	$3.57 \times 10^{-18} F/\mu m^2$	44.75%	186.2%	105.53%	99.32%	99.32%
	P+ Diff - NWELL	$1.92 \times 10^{-16} F/\mu m^2$	12.80%	124.1%	28.95%	24.81%	24.81%

Table 1: Global Individual Parameter Statistics

Electrical Parameters		Global Worst Case % Deviation	Largest Lot Worst Case % Deviation
Voltage Threshold	N:1.2/0.8	15.7%	9.03%
	P:1.2/0.8	14.2%	9.53%
Gain Factor	N:1.2/0.8	38.8%	12.35%
	P:1.2/0.8	31.4%	16.39%
Sheet Resistance	P+ Diff	31.6%	18.1%
	Poly	46.3%	37.96%
	Metal1	28.8%	10.85%
	Metal2	19.9%	8.0%
Line Width	Metal1	29.3%	9.16%
	Metal2	20.1%	5.21%
Contact Resistance	P+ Diff - Metal1	26.4%	14.2%
	Metal1 - Metal2	116.0%	70.11%
Area Capacitance	Metal2 - Metal3	41.9%	26.01%
	Poly - Metal2	26.9%	16.1%
	Metal1 - Metal2	30.0%	17.07%
	Metal1 - PWELL	36.5%	3.18%
	Metal2 - PWELL	55.2%	10.07%
Fringe Capacitance	P+ Diff - Poly	186.2%	31.62%
	P+ Diff - NWELL	124.1%	30.38%

Table 2: Largest Lot Individual Parameter Statistics

Electrical Parameters		Contact Resistance		Sheet Resistance		
		P+ Diff - Metal1	Poly - Metal1	P+ Diff	N+ Diff	Poly
Contact Resistance	N+ Diff- Metal1	0.4	0.7*	0.17	0.64*	0.48
	Poly - Metal1	0.43	-	0.39	0.56	0.62*
Sheet Resistance	P+ Diff	0.62*	0.39	-	0.25	0.41

Table 3: Correlation between resistance parameters

- Sheet Resistance: The deviations are in the following order:

  Poly > P+, N+ > M1 > M3

  The large variations in the Poly sheet resistance may be attributed to the varying degrees of resistivity induced by the siliciding process.

7.2.2 Largest Lot Inferences

The relative variations of the parameters within the largest lot taken as a population follows the same pattern as the relative variations of the parameters in the global population. It has also been observed that, for a given parameter, the deviations over a lot is generally greater than the deviations on a wafer which in turn is greater than the deviations across wafers at a particular coordinate on the wafer. In other words, referring to Figure 5, it has been observed that variations in Case 1 > variations in Case 3 > variations in Case 2.

7.3 Correlation Results

- The voltage threshold of the P and the N-channel transistors are uncorrelated.
- The correlation coefficient for the voltage threshold of P-channel transistors was found to be 0.64 under zero body-to-substrate voltages irrespective of the size of the transistors.
- The correlation coefficient for gain factors of P-channel transistors transistors was found to be 0.8.
- The correlation coefficient for gain factors of P and N-channel transistors was found to be 0.8.
- Contact resistances and sheet resistances have high correlation only among themselves as shown in Table 3.
- Area capacitances and fringe capacitances have high correlation only among themselves. These correlations are shown in Tables 4, 5 and 6.

7.4 Correlation Inferences

The positive correlation of the gain factors of the P and N transistors is attributed to the LDD process affecting the channel of both N and P transistors in the same manner.

Electrical Parameters		Area Capacitance		Fringe Capacitance	
		N+ Diff - PWELL	Poly - Metal1	N+ Diff - PWELL	P+ Diff - Poly
Area Capacitance	N+ Diff - Poly	−0.69*	−0.79*	0.72*	0.74*
Area Capacitance	N+ Diff - PWELL	-	0.64*	−0.88*	-

Table 4: Correlation between capacitance parameters: I

Electrical Parameters		Area Capacitance	
		PWELL - Poly	PWELL - Metal3
Area Capacitance	PWELL - Metal2	0.73*	0.76*

Table 5: Correlation between capacitance parameters: II

The contact resistances involving the a common diffusion layer are highly correlated. This is because the sheet resistance contributes to contact resistance because the sheet resistance estimation comprises of a distributed network involving the contact resistances. This explains the high correlation between the contact resistances and the sheet resistances involving diffusion layers. The high positive correlation between the Poly sheet resistance and the Poly-Metal1 contact resistance is due to the sheet resistance of Poly affecting both resistances in the same manner.

The high positive correlation between area capacitances P+ - Poly and N+ - Poly is possibly due to the fact that the dielectric between them is deposited in the same step. The correlation between the area capacitances poly-metal and metal-metal given in Table 6 is attributed to "neighborhood" effect i.e., these capacitances are influencing each other due to their test structures being in close proximity. Hence these correlations may be ignored.

8 Impact of Process Variations on Circuit Operation

In this section, we will illustrate the effect of the variations in the values of electrical parameters due to process variations on circuit operation. The results are obtained by simulation using PSPICE, and combinations of changes in electrical parameters are selected that are consistent with the correlations found and discussed in the previous sections. Three circuit aspects will be considered, viz., simple delay of a signal between two buffers, the delay due to crosstalk between two lines running parallel to each other ([3]), and the crosstalk pulse height due to

Electrical Parameters		Area Capacitance		
		Metal1 - Metal2	Metal2 - Metal3	Metal1 - Metal3
Area Capacitance	Poly - Metal2	0.88*	-	-
Area Capacitance	Poly - Metal3	-	0.87*	0.96*
Area Capacitance	Metal1 - Metal3	0.82*	0.87*	-

Table 6: Correlation between capacitance parameters: III

mutual capacitive coupling between two parallel lines ([6]). The relevance of the correlations between parameters to the choice of design corners is demonstrated with a simple example involving transistor gain factor. Throughout this section any reference to the extremum values of a parameter always means the value of the parameter given by its mean$\pm x$% beyond which there are still 2% of the data points (actually the values correspond to the mean$\pm x$% where x is the entry in the 4th column of Table 1).

8.1 Effect of Process Variations

The three examples that demonstrate the impact of process variations on the circuit parameters are described in the following subsections. The inference to be drawn from these experiments is given after these examples are described.

8.1.1 Simple Delay

The circuit used to study delay is shown in Figure 8, and consists of one inverter driving another inverter through Metal1 interconnect. The sizes of the transistors in the inverters and the length of the metal interconnect are chosen to obtain a realistic nominal driver output rise time of 130ps. This is reasonable assuming a clock period of 4ns.

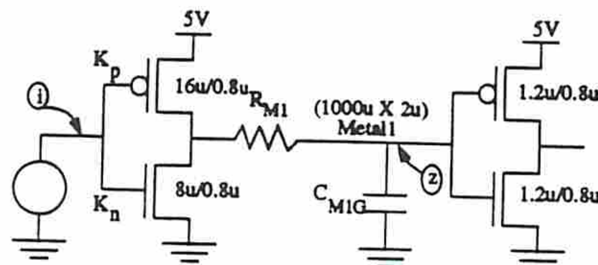


Figure 8: Experimental Setup for Simple Delay

The resistance of the metal interconnect is calculated from its dimensions and the average value of resistance per unit square for Metal1 obtained from the process data. The Metal1 to substrate capacitance is determined in a similar manner. The electrical parameters for the transistor, viz., process gain factor and voltage threshold, used in the PSPICE model are initially set to the average values obtained from the process data. For simplicity, only the delay in the rising transition at the input of the load inverter is considered. Also, the contact resistances between the diffusion and metal, and between metal and the poly layers are ignored since they are numerically insignificant compared to the interconnect resistance.

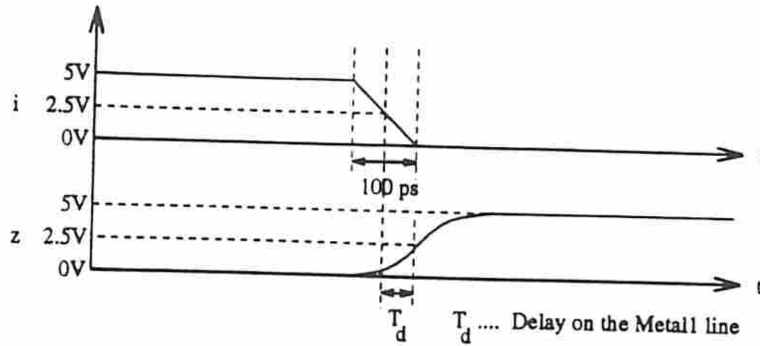


Figure 9: Waveforms for Simple Delay

Circuit Parameter	Mean Delay Value (ps)	Minimum Delay		Maximum Delay	
		Value (ps)	% Deviation from Mean	Value (ps)	% Deviation from Mean
Simple Delay	156.2	124.8	20.1	199.6	27.78

Table 7: Variations in Simple Delay

First the case using the average electrical values is considered. Then, the maximum and minimum delay values that are obtainable through process variations are measured by choosing extremum values for parameters from the process variations that excite the worst case behavior. For the simple delay case, to obtain the maximum possible delay value, the minimum value of gains K_p and K_n for the driver transistors and the maximum value of the capacitance between the Metal1 interconnect to substrate (C_{M1G}) are chosen while the other parameters retained their average values. Since the delay was found to be insensitive to the variations in interconnect resistance because of the high driver strength, the resistance of the interconnect is also retained at its average value. For the same reason, the threshold voltages of the transistors were maintained at their average values. The waveforms at the input and output probe points are shown in Figure 9.

The delay values thus obtained are shown in Table 7. A variation of about 25% in the delay was observed. It was also observed that the delay is primarily influenced by the interconnect to substrate capacitance.

8.1.2 Crosstalk Delay

To study the impact of crosstalk on signal delay we employed a circuit consisting of two sets of driver-load inverters (each one similar to the circuit shown in Figure 8) whose interconnects are coupled through mutual capacitance. One of the drivers is larger

than the other and drives a longer line ($4000\mu \times 4\mu$) and serves the purpose of inducing crosstalk in the other interconnect. The stronger driver drives a long Metal2 interconnect while the weaker driver drives a relatively short ($1000\mu \times 2\mu$) Metal1 interconnect. The circuit along with the dimensions of the components is given in Figure 10. As before, the interconnect re-

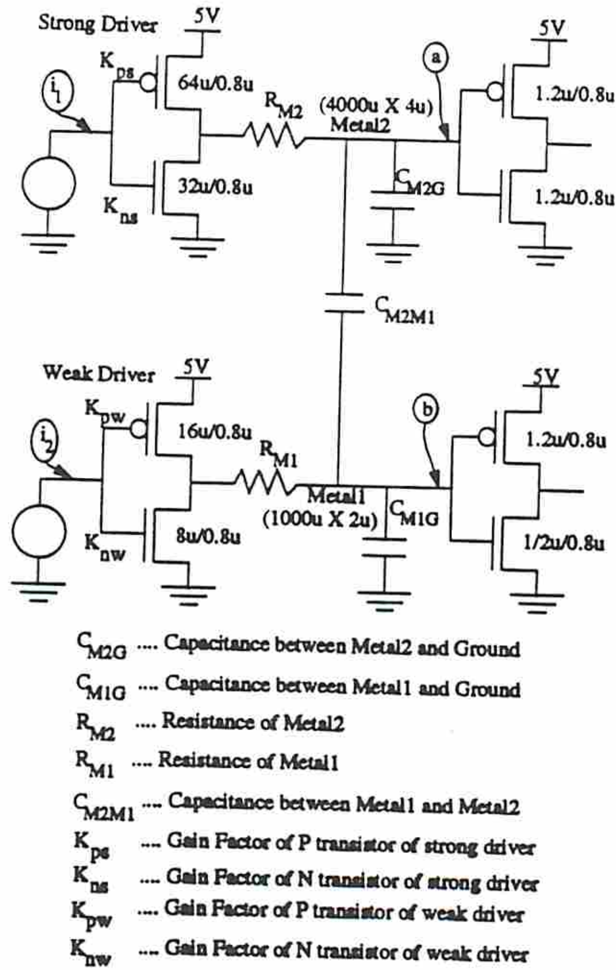


Figure 10: Experimental Setup for Crosstalk Effects

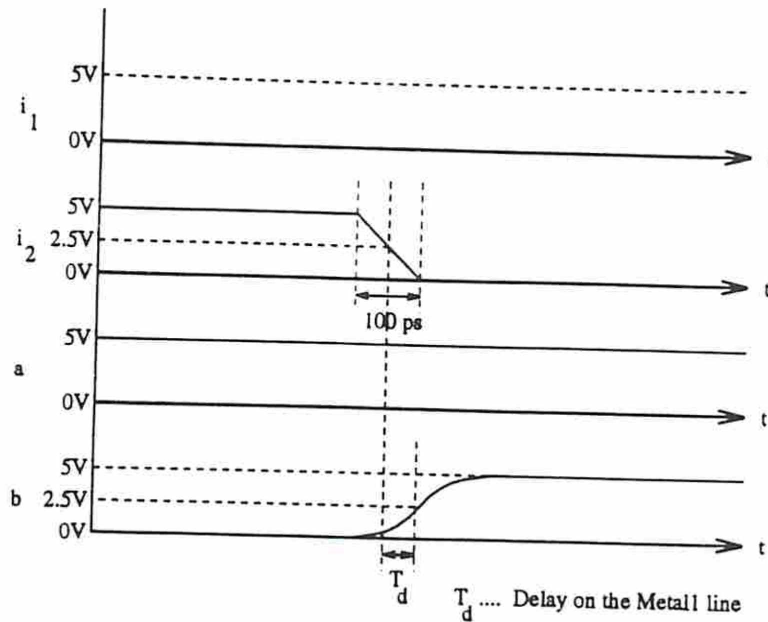


Figure 11: Waveforms for Case 1 of Crosstalk Delay

sistance and capacitance are calculated using their feature sizes and nominal values from the process data.

The delay of a signal arriving at the load of the weaker driver is influenced by the mutual capacitive coupling and by the type of transition that occurs at the stronger driver. This gives rise to three cases of delay due to crosstalk. The first case occurs when there is no transition at the strong driver while there is a rising transition at the output of the weak driver and is shown in Figure 11. The second case arises due to opposite transitions on the two interconnects and is shown in Figure 12. The third case arises due to identical transitions on the two interconnects and is shown in Figure 13. For simplicity, only the delay of a rising transition at the load of the weak driver is considered throughout this paper.

The nominal delay values are measured for each of the three cases mentioned above using the nominal values for all parameters. Then the worst case behaviors (maximum and minimum delay) are excited by using the extremum values for each parameter that create the worst case. For the first case, the minimum delay behavior was excited by choosing the maximum gain value for the driver transistors, the minimum Metal1 to substrate capacitance (C_{M1G}), and the minimum mutual capacitance between the metal interconnects (C_{M2M1}). These are reversed to the opposite extremum values to obtain the maximum delay behavior. For

the second and third cases, the minimum delay behavior is obtained by selecting the minimum mutual capacitance between the interconnects (C_{M2M1}), the minimum interconnect to substrate capacitances (C_{M1G} and C_{M2G}), and the maximum gain values (K_{ps}, K_{ns}, K_{pw} and K_{nw}) for both the strong and weak driver transistors. As before, the maximum delay behavior is obtained by reversing these parameter values to their other extremums. The variations in the resistance of the interconnects do not have any significant impact on the results and hence the average values

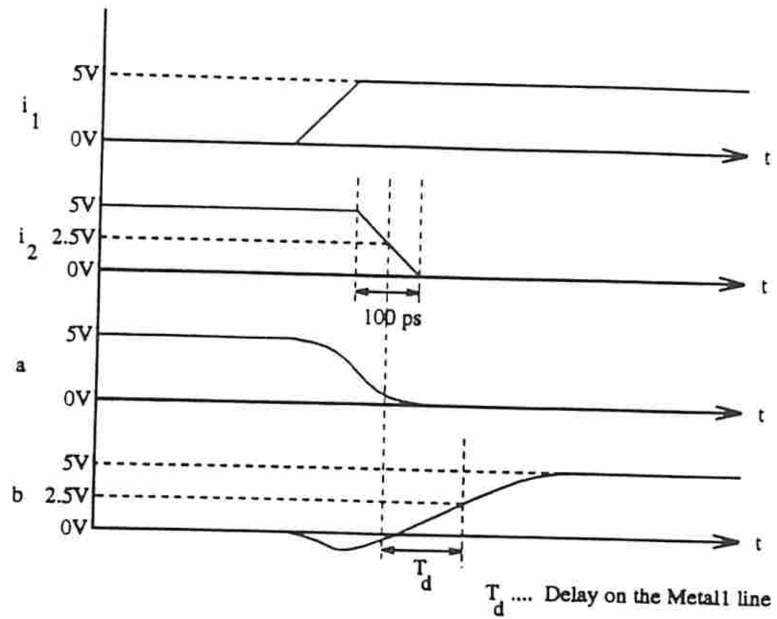


Figure 12: Waveforms for Case 2 of Crosstalk Delay

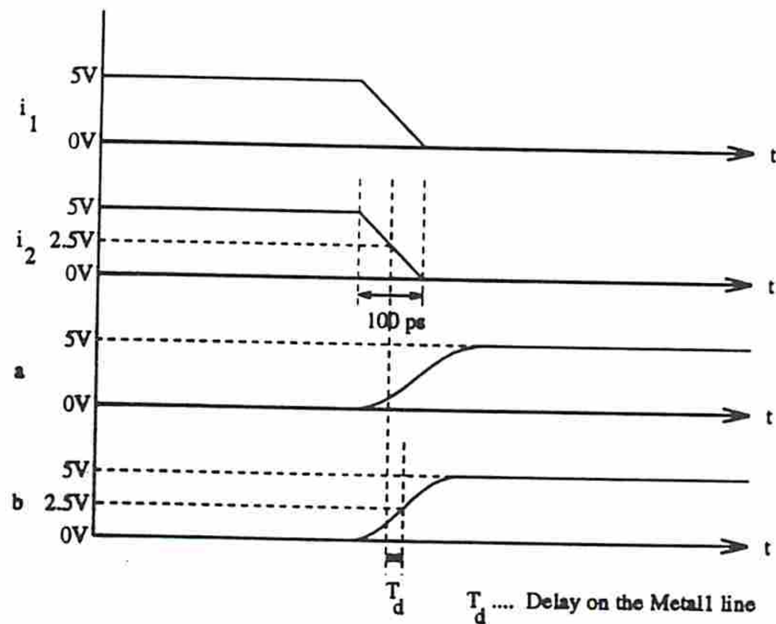


Figure 13: Waveforms for Case 3 of Crosstalk Delay

Circuit Parameter	Mean Delay Value (ps)	Minimum Delay		Maximum Delay	
		Value (ps)	% Deviation from Mean	Value (ps)	% Deviation from Mean
Crosstalk Delay: Case 1	217.3	177.4	18.36	269.5	24.02
Crosstalk Delay: Case 2	315.0	248.0	21.27	400.0	26.98
Crosstalk Delay: Case 3	165.5	128.2	22.54	205.7	24.29

Table 8: Variations in Crosstalk Delay

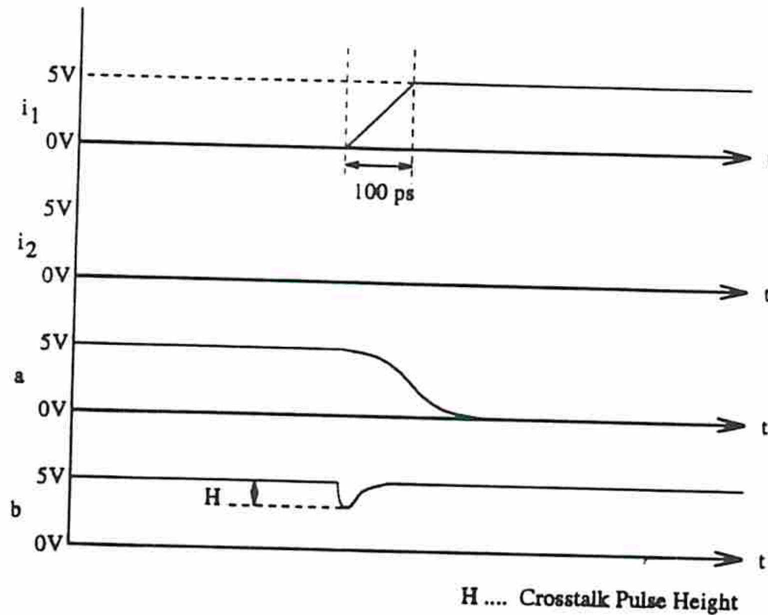


Figure 14: Waveforms for Crosstalk Pulse Height

for these parameters are used.

The delay values obtained are shown in Table 8. The delay is found to vary by 25% around its mean value. Here again, the interconnect capacitance to ground, the mutual capacitance between interconnects and the strengths of the two drivers and hence their variations strongly influence the variations in the delay.

8.1.3 Crosstalk Pulse Height

The circuit shown in Figure 10 was also used to study the variation in the crosstalk pulse height. The height of the crosstalk pulse is measured by setting up a falling transition at the load of the stronger driver and keeping the load of the weak driver charged at 5V.

The falling transition at the load of the stronger driver induces a pulse on the interconnect at the load of the weak driver due to mutual capacitive coupling. The height of this pulse varies about a nominal value as the parameters of the circuit change due to process variations. The crosstalk pulse is illustrated in Figure 14.

The maximum pulse height is obtained by selecting the minimum line width for Metal2

Circuit Parameter	Mean Height Value (V)	Minimum Height		Maximum Height	
		Value (V)	% Deviation from Mean	Value (V)	% Deviation from Mean
Pulse Height	0.6465	0.4291	33.63	0.9333	44.36

Table 9: Variations in Crosstalk Pulse Height

interconnect and the maximum line width for Metal1 interconnect. This was done to increase the overlap area of the mutual capacitance between the interconnects. In addition, the minimum values for the interconnect-to-substrate capacitances (C_{M1G} and C_{M2G}), the minimum values for the interconnect resistances (R_{M1} and R_{M2}), the maximum values for the gain factor (K_{ps}, K_{ns}, K_{pw} and K_{nw}) for the drivers, and the maximum value for the mutual capacitance between the interconnects (C_{M2M1}) were chosen. The minimum height of the pulse was obtained by choosing the opposite extremums of the above parameters.

The pulse height values thus obtained are shown in Table 9. The height of the pulse is found to vary by about 40% around its average value.

8.1.4 Inferences

These examples demonstrate that there are significant variations about the average value of simple delay, crosstalk delay and crosstalk pulse height due to process variations. It has been shown that parameters that were traditionally considered significant, such as the gate load capacitance are of lesser importance compared to the interconnect-to-substrate capacitance and the mutual capacitance between lines, since the impact of the variations on these parameters due to the process are much more than that of the variations on the gate-to-substrate capacitance. The importance of considering the effects of process variations during design is further emphasized by the fact that the parameters that excite the worst case behavior, such as interconnect-to-ground capacitance and mutual capacitance between interconnects, are not, in the current scenario, being considered while designing the circuit. Hence, ignoring variations in these parameters is detrimental to yield, especially in high speed deep sub-micron circuits where process variations are expected to be considerable.

8.2 Effect of Correlations

The existence of correlations between electrical parameters is useful in discarding "fictitious" design corners that never occur in practice, and hence aid in identifying aggressive design styles that lead to correct circuit operation. Moreover, in addition to the fact that fictitious corners can be discarded, new design corners can be shown to emerge from within the design space that were hitherto not considered.

A simple example is used to demonstrate this idea. For the case discussed in section 8.1.3, the height of the crosstalk pulse has been shown [6] to be proportional to K_{ns}/K_{pw}. If the height of the worst case crosstalk pulse is to be estimated, it is quite natural to assume the maximum possible value of K_{ns} and the minimum possible value of K_{pw}. From the MOSIS data for the gain factors, the maximum value for K_{ns} is $6.2811 \times 10^{-5} A/V^2$ and the minimum value for K_{pw} is $1.3133 \times 10^{-5} A/V^2$. Hence, a design corner corresponding to $K_{ns}/K_{pw} = 4.783$ would be

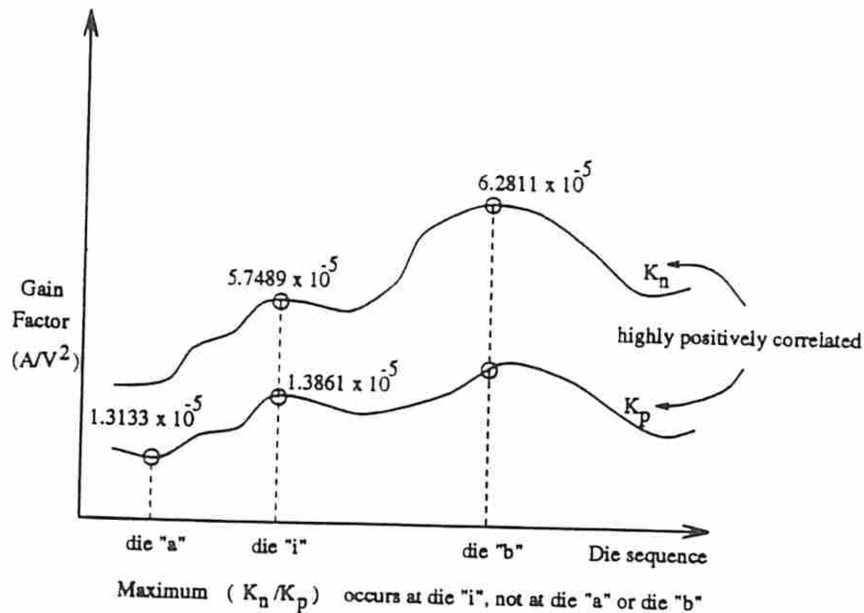


Figure 15: Example of redefined corners due to correlation

predicted. However, since K_{ns} and K_{pw} are highly correlated (section 7.3), K_{ns} and K_{pw} increase or decrease together. Hence, the situation where K_{ns} is maximum and K_{pw} is minimum does not arise at the same time. In fact, the data set shows that this is indeed the case. Thus such a combination of K_{ns} and K_{pw} values gives rise to a fictitious design corner. However, the ratio of K_{ns}/K_{pw} is in fact maximized for another pair of K_{ns} and K_{pw} values, viz., $5.7489 \times 10^{-5} A/V^2$ and $1.3861 \times 10^{-5} A/V^2$ respectively with a maximum value of 4.147. It has to be noted that none of the above two values for K_{ns} and K_{pw} are extremum values. Hence, the new design corner now lies in the hitherto unexplored design space. (In fact, the word corner is a misnomer since this point is internal to the design space.) Figure 15 illustrates this concept where each vertical pair of gain factors correspond to a different die.

9 Conclusion

Statistical analysis on the electrical parameters obtained by measurement on the wafers of a 0.8 μm process showed significant deviations of these parameters from their nominal values due to the process variations. It has also been observed that many of these parameters are correlated. It has been shown through three examples that parameters that were long considered inconsequential as far as circuit design is concerned have now assumed significance due to the impact of their variations on the performance of a circuit. This necessitates a tighter coupling between the areas of fabrication and circuit design. Also, the presence of correlations between parameters facilitates the identification and removal of fictitious design corners thus leading to more aggressive designs. These results also lead to the identification of real design "corners" that may lie in areas of the hitherto unexplored design space. The results of this analysis point to new areas of concern to

design, validation and test engineers.

10 Acknowledgement

We would like to thank the Information Sciences Institute of the University of Southern California, and in particular Wes Hansford and Dr. Vance Tyree for making the MOSIS data available to us, for answering numerous questions on how to process the data, and for helping in the interpretation of our results. We would like to thank Wei-Yu Chen for his help in designing the experiments and analyzing the results.

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Appendix I

The list of parameters measured are given below.

Voltage Threshold

The voltage threshold of transistors of the following device sizes and body-to-substrate bias voltages are measured.

```
N:  W=1.20:  L=0.8:  VBS=-0.0V
N:  W=7.20:  L=0.8:  VBS=-5.0V
N:  W=7.20:  L=0.8:  VBS=-2.5V
N:  W=7.20:  L=0.8:  VBS=-0.0V
N:  W=48.0:  L=0.8:  VBS=-0.0V
N:  W=1.20:  L=1.2:  VBS=-0.0V
N:  W=2.00:  L=1.2:  VBS=-0.0V
N:  W=3.20:  L=1.2:  VBS=-0.0V
N:  W=5.20:  L=1.2:  VBS=-0.0V
N:  W=7.20:  L=1.2:  VBS=-0.0V
N:  W=7.20:  L=2.0:  VBS=-0.0V
N:  W=7.20:  L=3.2:  VBS=-0.0V
N:  W=7.20:  L=5.2:  VBS=-0.0V
N:  W=7.20:  L=7.2:  VBS=-5.0V
N:  W=7.20:  L=7.2:  VBS=-2.5V
N:  W=7.20:  L=7.2:  VBS=-0.0V
P:  W=1.20:  L=0.8:  VBS=+0.0V
P:  W=7.20:  L=0.8:  VBS=+5.0V
P:  W=7.20:  L=0.8:  VBS=+2.5V
P:  W=7.20:  L=0.8:  VBS=+0.0V
P:  W=48.0:  L=0.8:  VBS=+0.0V
P:  W=1.20:  L=1.2:  VBS=+0.0V
P:  W=2.00:  L=1.2:  VBS=+0.0V
P:  W=3.20:  L=1.2:  VBS=+0.0V
P:  W=5.20:  L=1.2:  VBS=+0.0V
P:  W=7.20:  L=1.2:  VBS=+0.0V
P:  W=7.20:  L=2.0:  VBS=+0.0V
P:  W=7.20:  L=3.2:  VBS=+0.0V
P:  W=7.20:  L=5.2:  VBS=+0.0V
P:  W=7.20:  L=7.2:  VBS=+5.0V
P:  W=7.20:  L=7.2:  VBS=+2.5V
P:  W=7.20:  L=7.2:  VBS=+0.0V
```

The histograms and sequence plots of voltage threshold have the acronym VTH in their title followed by number that corresponds to their location in the above listing.

The width of the 48 um transistor, however, had been changed during the middle of the year to 25 um and hence measurements on those were not used to make inferences.

Gain Factor

The gain factor is measured for the same list of transistors given above under the same bias conditions. The histograms and sequence plots of gain factor have the acronym GF in their title followed by number that corresponds to their location in the above listing.

Sheet Resistance and Line Width

The sheet resistance and line width of the following materials are measured:

```
P+DF
N+DF
MET1
MET3
POLY
MET2
```

The histograms and sequence plots of sheet resistance have the acronym SR in their title followed by number that corresponds to their location in the above listing. The line width plots use the acronym LW.

Contact Resistance

The contact resistances of the following contacts are measured:

```
LL=N+        UL=METAL1  VIA
LL=N+        UL=METAL1  CUT
LL=POLY      UL=METAL1  VIA
LL=POLY      UL=METAL1  CUT
LL=P+        UL=METAL1  VIA
LL=P+        UL=METAL1  CUT
LL=METAL1    UL=METAL2
LL=METAL2    UL=METAL3
```

Here LL is the lower layer and UL is the upper layer of the contact. The histograms and sequence plots of sheet resistance have the acronym CR in their title followed by number that corresponds to their location in the above listing.

Area Capacitance

The following area capacitances are measured:

```
P+ACTIVE  POLY
N+ACTIVE  POLY
NWELL     P+ACTIVE
PWELL     N+ACTIVE
PWELL     POLY
PWELL     METAL1
PWELL     METAL2
PWELL     METAL3
METAL1    METAL2
METAL2    METAL3
METAL1    METAL3
POLY      METAL1
POLY      METAL2
POLY      METAL3
```

The histograms and sequence plots of sheet resistance have the acronym AC in their title followed by number that corresponds to their location in the above listing.

Fringe Capacitance

The following fringe capacitances are measured:

```
NWELL    P+ACTIVE
PWELL    N+ACTIVE
P+ACTIVE POLY
N+ACTIVE POLY
```

The histograms and sequence plots of sheet resistance have the acronym FC in their title followed by number that corresponds to their location in the above listing.

Appendix II

Representative plots for the two types of graphs are given in this appendix from Figure 16 to Figure 27. As an example, the first pair of graphs shown are for voltage threshold of an N channel transistor with $W = 1.2\mu$m and $L = 0.8\mu$m and body to substrate voltage is 0. Figure 16 shows a histogram of voltage threshold values with the title showing the parameter, the mean, the percentage standard deviation, and the worst case percentage deviation. Figure 17 shows an example of a sequence plot that shows the voltage threshold values sorted within each wafer lot and arranged in lot sequence. Also, the plots that correspond to the global data set have the label GLOBAL in their title to distinguish them from the plots for the largest single lot.

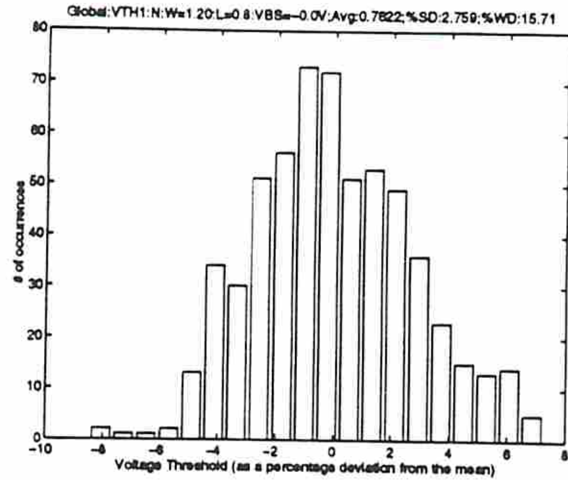

Figure 16: Representative histogram for Voltage Threshold

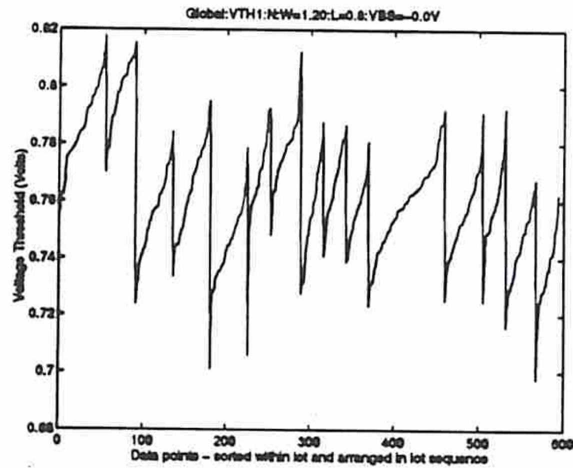

Figure 17: Representative sequence plot for Voltage Threshold

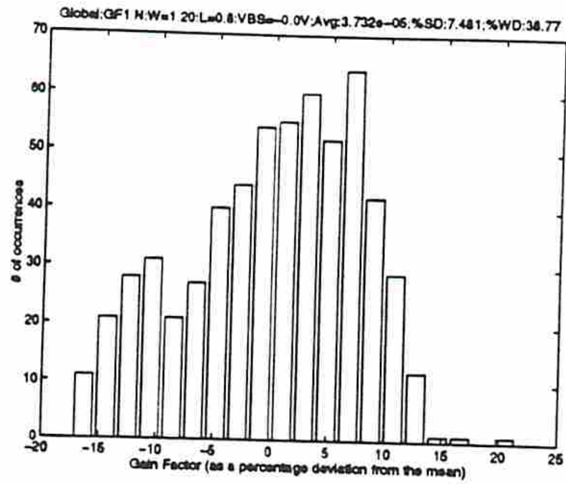

Figure 18: Representative histogram for Gain Factor

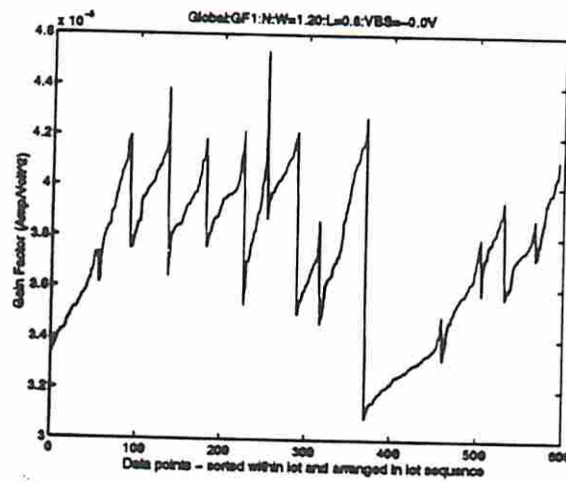

Figure 19: Representative sequence plot for Gain Factor

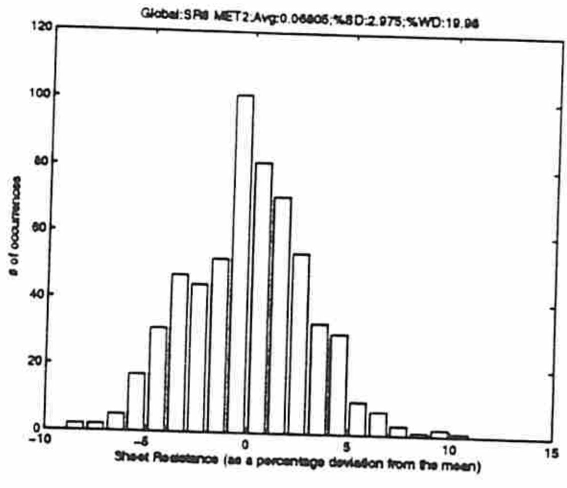

Figure 20: Representative histogram for Sheet Resistance

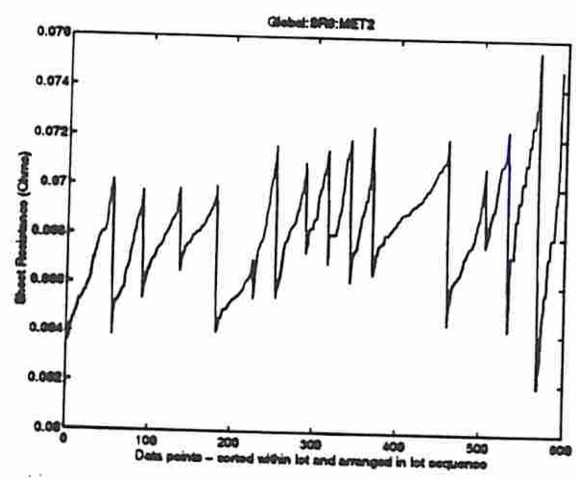

Figure 21: Representative sequence plot for Sheet Resistance

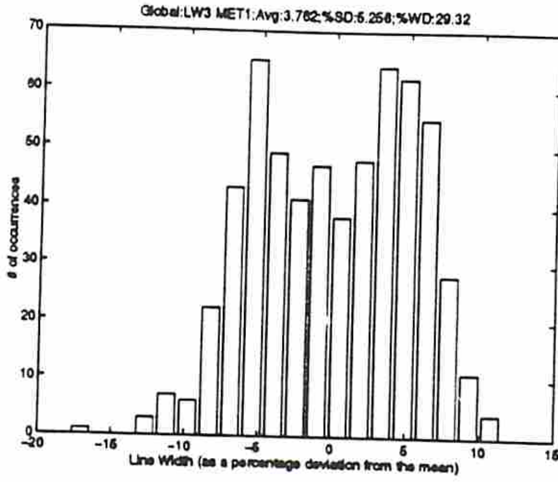

Figure 22: Representative histogram for Line Width

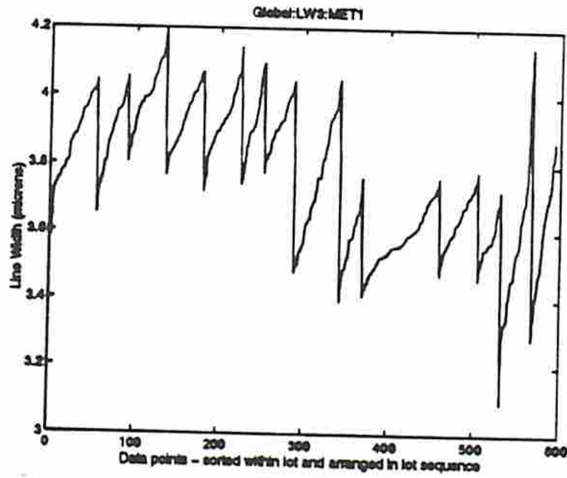

Figure 23: Representative sequence plot for Line Width

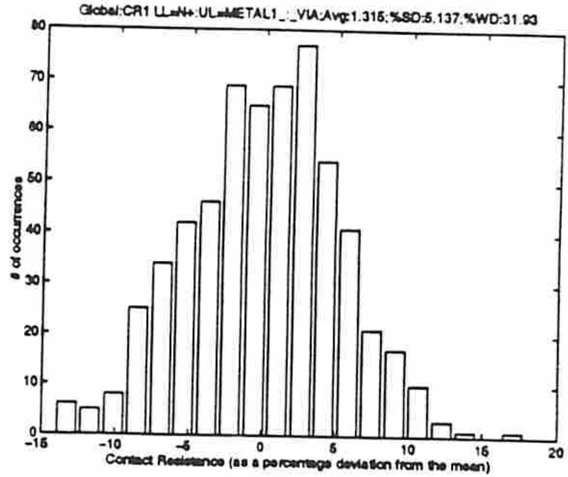

Figure 24: Representative histogram for Contact Resistance

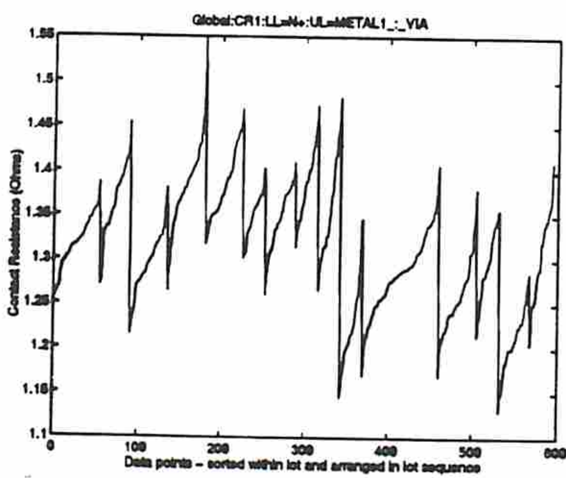

Figure 25: Representative sequence plot for Contact Resistance

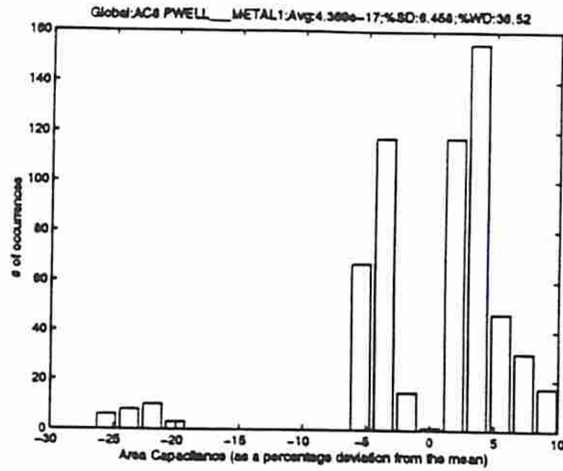

Figure 26: Representative histogram for Area Capacitance

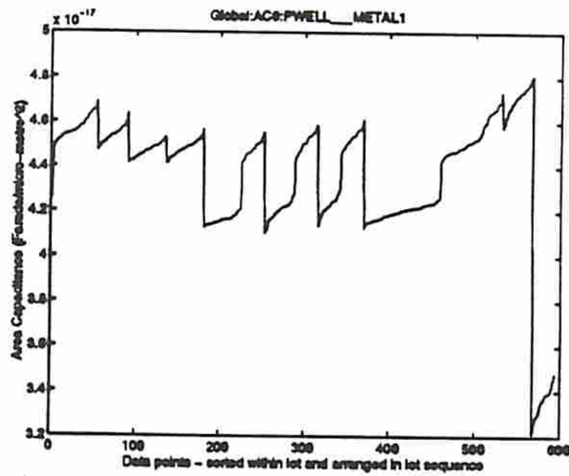

Figure 27: Representative sequence plot for Area Capacitance