Structural Delay Testing Under Restricted Scan of Latch-based Pipelines with Time Borrowing

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Abstract

High-speed circuits use latch-based pipelines in some of their most delay-critical parts. For latch-based pipelines, the path delay fault coverage provided by the classical approaches is often abysmally low and none of the classical design-for-testability (DFT) approaches can be used to simplify delay testing or to improve coverage. In [1], we presented the first DFT approach for delay testing of such pipelines.

*In this paper, we have developed a new theoretical framework that provides high robust delay fault coverage at low DFT overheads. We have also developed a new test generation approach that exploits this theory and **any** set of available DFT configurations to provide the corresponding maximum coverage for any scenario of time borrowing – expected as well as unexpected. We demonstrate the benefits of the proposed approach via extensive experiments.*

1. Introduction

Extensive pipelining partitions large logic blocks into smaller blocks. Consequently logic paths within a block become shorter and the task of path delay testing *may* become easier and higher robust path delay coverage *may* be obtained. Such simplifications of delay testing do occur when flip-flops are used for pipelining. However, in many high-speed parts of circuits, latches are used for pipelining to obtain higher performance, via skew tolerance and intentional time borrowing [5], as well as higher yields at higher performance levels, via unintentional time borrowing. Latch-based pipelining makes the task of path delay testing more complicated. In particular, it makes it necessary to target multi-block paths. Consequently, the number of paths to be tested and their lengths both remain high, and robust coverage remains low. Furthermore, none of the classical DFT approaches can be used to simplify delay testing or to improve coverage [1].

In our earlier work [1], we proposed the first DFT-based approach for robust path delay testing of such circuits. That approach suffered from high overheads, due to replacement of latches by scan cells, routing a large number of DFT control signals, and complicated scan chain designs that could be reconfigured to support a large number of DFT configurations.

In this paper, we derive new results that require drastically lower number of latch configurations – $O(k)$ instead of $O(2^k)$ for a two-stage pipeline with k latches between the stages – while guaranteeing equally high robust path delay coverage. This reduces all overheads due to DFT. Furthermore, even for cases where only a fraction of these $O(k)$ configurations (or any other set of configurations, for that matter) are available, we have developed an approach that helps attain the corresponding maximum coverage. This is especially useful since it allows us to avoid DFT configurations that significantly degrade circuit performance. We present a new test generation approach that uses all our theory along with **any** given set of available DFT configurations, and generates tests that provide the corresponding maximum robust coverage for any scenario of time borrowing.

We have applied our approach to a number of circuits assuming different sets of available DFT configurations and for a number of different time borrowing scenarios. The results clearly demonstrate that the proposed approach can provide high robust coverage while using significantly fewer DFT configurations.

This paper is organized as follows. Section 2 identifies the key challenges in path delay testing of latch-based pipelines. Section 3 presents our new theoretical framework. Section 4 presents the proposed test generation approach and Section 5 presents the experimental results. Finally, we conclude in Section 6.

2. Key Challenges and Previous Work in Delay Testing of Latch-based Pipelines

Time borrowing [5] may be *intentional* if it is planned during the design of a circuit. Also, time borrowing may occur *unintentionally* if delay variations and/or delay defects during fabrication cause such borrowing at some latches in some fabricated copies of the circuit. Hence, the sites of unintentional time borrowing vary from one fabricated chip to another. Even in the case of intentional time borrowing, the precise amount of time borrowed at a latch for any particular vector is not known *a priori* and depends on the delay variations and delay defects.

Hence, it is impossible to use scan-in mode of a latch without knowing whether the latch is a site of time borrowing. Furthermore, when time borrowing is known to occur, it is practically impossible to use scan to apply

tests where bits are precisely skewed to replicate the amount of time borrowed, which is different for each test and for each copy of the chip. Hence, if a latch is a site of time borrowing, it is necessary to test *multi-block paths*, i.e., paths obtained by concatenating appropriate paths in successive logic blocks separated by latches. Since many latch-based parts of circuits (e.g., data-paths) contain astronomical number of such *multi-block paths* [3], the classical test approach, which targets the entire pipeline, typically suffers from impractically high test generation complexity, high test application time, and for many circuits, meaninglessly low fault coverage. Hence, the use of some new type of DFT is imperative in order to reduce test generation and test application times significantly while providing meaningfully high values of fault coverage by targeting shorter paths.

3. Developing a Structural Delay Test – Latch-based Analysis

3.1 Basic assumptions

In this paper, every latch is assumed to be a positive D-latch (i.e., it becomes transparent when the *corresponding clock* is high). For simplicity of analysis, complementary clocks are used. However, the approach is applicable to any type of clocks, including two-phase non-overlapping, four-phase non-overlapping, and four-phase overlapping [5]. To simplify the discussion, all latches are assumed to be ideal latches where all delays as well as the setup and hold times are zero. However, our approach for test development inherently takes into account the characteristics of real latches. Also, the characteristics of real latches are explicitly considered during the detailed design of DFT circuitry.

A latch may operate in the following four modes.

(1) *Normal mode*: The latch is transparent when the corresponding clock is high and holds its state when the clock is low.
(2) *Scan-in mode*: Vectors are loaded via scan-in and applied at the rising edge of the corresponding clock.
(3) *r-capture scan-out mode*: The latch captures response at the rising edge of the corresponding clock for scan out.
(4) *f-capture scan-out mode*: The latch captures response at the falling edge of the corresponding clock for scan out. (This mode is not used in this paper.)

Time borrowing is assumed not to occur at the "primary" inputs and outputs of the entire latch-based circuit. This is very often the case because high-speed latch-based pipelines are typically embedded in larger circuits that are otherwise flip-flop based. We may test blocks individually. Alternatively, we may test any set of contiguous blocks together as a single entity. In either case, we use the term *sub-circuit under test (SCUT)* to describe the block(s) under test during a particular phase.

In order to formulate a general approach for structural delay testing for latch-based high-speed pipelines, we start with a latch-by-latch analysis. First, the latches where time borrowing occurs and the latches where time borrowing does not occur are separately considered. In each case we discuss how to test the paths associated with the latch and what mode of operation of the latch to use, depending on whether the latch is on-path (a part of the target multi-block path) or off-path (any connection to a gate along the target path is via one of its off-path inputs). In these analyses, two new techniques are introduced that provide high test quality without requiring any additional DFT hardware.

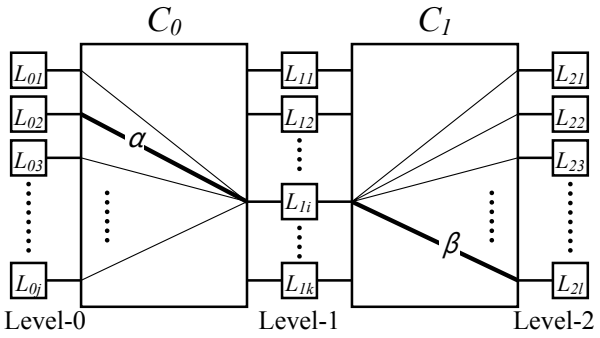


Figure 1 A two-stage linear pipeline

In this section, for simplicity of explanation, the discussion is based on the two-stage linear pipeline shown in Figure 1. However, the ideas developed are applicable to general latch-based linear pipelines as well as to general latch-based networks. Assume that there are j latches at the inputs of the first combinational logic block C_0 (level-0 latches), k latches between C_0 and C_1 (level-1 latches), and l latches at the outputs of C_1 (level-2 latches).

3.2 Test of the first stage ($SCUT_0$)

As illustrated in [1], since classical methods must test the entire circuit (C_0 and C_1 jointly) without any DFT support in level-1 latches, they suffer from excessive test generation and test application times and, for many circuits, abysmally low fault coverage. However, [1] first introduced the basic idea of structural delay testing of such circuits where DFT circuitry is used adaptively depending on the sites of time borrowing in the circuit.

Similar to the approach described in [1], the first logic block C_0 is tested by itself by operating level-0 latches in scan-in mode and level-1 latches in r-capture scan-out mode. The purpose of this test is to identify the level-1 latches that are sites of time borrowing. Assume that such testing detects time borrowing at a subset of level-1 latches, which is denoted by the set L^{TB},

$L^{TB} = \{L_{1i} \mid L_{1i}$ is a site of time borrowing, $1 \le i \le k\}$.

The rest of the level-1 latches, that are not sites of time borrowing, constitute a set L^{NTB}, *i.e.*,

$L^{NTB} = \{L_{1i} \mid L_{1i}$ is not a site of time borrowing, $1 \le i \le k\}$.

After testing the first stage by itself ($SCUT_0$), we target the multi-block paths that span C_0 and C_1. The following two sections deal with these multi-block paths by considering the level-1 latches that are sites of time borrowing.

3.3 Test of multi-block paths via latches at which time borrowing occurs

In order to test multi-block paths that pass via a latch $L_{1i} \in L^{TB}$, scan-in mode cannot be used for the latch L_{1i}, since no known DFT circuitry can replicate appropriately skewed test application and response capture corresponding to the precise amount of time borrowing, which varies from vector to vector and from one fabricated copy of chip to another. Therefore, *only normal mode can be used at time borrowing latch L_{1i} for testing multi-block paths that pass via the latch*.

Suppose a multi-block path p that passes via $L_{1i} \in L^{TB}$ is targeted. As stated above, L_{1i} must operate in normal mode to test p. Now let us consider two alternatives that differ in the configuration of the other level-1 latches.

Alternative 1: All latches in level-1 are set to normal mode. Hence, p is targeted by using scan-in mode for level-0 latches and scan-out mode for level-2 latches.

Alternative 2: L_{1i} is in normal mode, a subset of the other level-1 latches are also in normal mode, and all the other level-1 latches are in scan-in mode.

By comparing the two alternatives, we obtain the following results.

Theorem 1 (Test quality): Any robust test for the multi-block path p using Alternative 2 invokes a delay equal to or greater than the delay of p. Hence, both alternatives enable testing of p with equal quality.

Proof: Let the target multi-block path p be comprised of sub-paths α and β, *i.e.*, the parts of p which fall in C_0 and C_1, respectively. Note that α ends at the input of on-path latch, L_{1i}, while β starts at the output of L_{1i}.

Since both alternatives use scan at all level-0 latches, the propagation of transition along α is identical in both cases. Furthermore, since the on-path level-1 latch, L_{1i}, is in the normal mode in both alternatives, the transition at the output of L_{1i}, *i.e.*, at the input of sub-path β, arrives in an identical manner in both alternatives. Note that if different tests are applied at level-0 latches in the two alternatives, the arrival time at the output of the on-path latch, L_{1i}, *i.e.*, at the input of sub-path β, may be different. However, due to the nature of robust tests, in each case, the delay invoked for α and via L_{1i} will be guaranteed to be equal to or greater than the worst-case delay of sub-path α plus the delay via the on-path latch L_{1i}. (This is a basic property attributed to robust tests. It is strictly true under some commonly used delay models. More details can be found in [7].)

Next consider the propagation of the transition along the sub-path β. The only difference between the two alternatives is in the values applied at off-path level-1 latches. However, since robust tests are applied in both alternatives, the propagation of transition along β will invoke a delay equal to or greater than that of β (again, due to the above property of robust tests).

Hence, we can conclude that in both alternatives, any robust test for the target path invokes a delay equal to or greater than that of the target path. ■

Theorem 2 (Coverage): If a multi-block path p is testable in Alternative 1, then it is testable in Alternative 2.

Proof: All conditions for robust detection of target path p can be expressed in terms of values required at on-path lines and at off-path inputs. Any vector that satisfies all these conditions is a robust test for p. Note that the conditions for robust detection of p are identical for the two alternatives.

In Alternative 2, we can specify independent logic values at all level-0 latches as well as at all level-1 latches that are scanned. In contrast, in Alternative 1, we can specify independent logic values only at all level-0 latches. (The values at all level-1 latches are implied by the values applied at the level-0 latches and the logic block C_0.) Hence, Alternative 2 provides a superset of value assignments to satisfy the conditions for robust detection for p. Consequently, if a robust test exists for p in Alternative 1, then one surely exists in Alternative 2. ■

In other words, Theorem 1 implies that the test quality obtained by any robust test applied using Alternative 2 is equal to the test quality obtained by any robust test applied using Alternative 1. Theorem 2 implies that robust delay fault coverage for Alternative 2 is definitely equal to and may be superior to that for Alternative 1.

Note that in Alternative 2, *any latch other than L_{1i} via which the targeted multi-block path p passes can be configured in scan-in mode, independent of whether or not the latch is a site of time borrowing*. This is due to the following two reasons. First, if a static value is applied via scan, time borrowing status of the latch has no impact on the on-path delay. Second, even if a rising or a falling transition is applied via scan, a robust test for a path does not require off-path transitions to satisfy any specific timing requirement. (In particular, an early off-path transition cannot reduce the on-path delay. In our scheme, the off-path transition is never later than in the normal mode.) Hence, even for a latch at which time borrowing is proven to occur, scan-in mode operation does not violate the robust delay test conditions, provided the latch is off-path.

Theorem 1 and Theorem 2 demonstrate that Alternative 2 is better for testing paths via lathes at which time borrowing occurs, provided that the DFT circuitry allows those latches to be configured in scan-in mode. If that is the case, it is necessary to consider the relationships among $(2^{k-1} - 1)$ configurations that conform to Alternative

2. Suppose there are two different configurations Alt-2a and Alt-2b of Alternative 2, such that the set of latches configured in scan-in mode in Alt-2a, S_1, is a proper subset of the set of latches in scan-in mode in Alt-2b, S_2, *i.e.,* $S_1 \subset S_2$. Recall that in both cases, the on-path latch, L_{1i}, is in normal mode. Similar to Theorems 1 and 2, we have the following results for Alt-2a and Alt-2b.

Theorem 3 (Coverage): If a multi-block path p is testable in Alt-2a, then it is testable in Alt-2b.

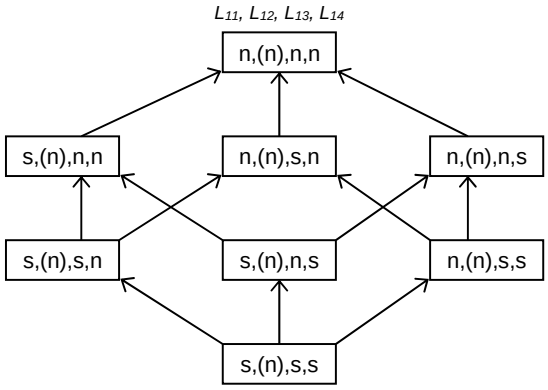
Proof: The proof is based on similar arguments as the proof for Theorem 2. ■

This result indicates that if we can use the scan configuration supported in Alt-2b to target a multi-block path p, then we need not use the scan configuration given by Alt-2a to test the path.

The following result is a corollary to Theorems 1 through 3.

Corollary 1: In testing of a multi-block path via a latch at which time borrowing is known to occur, the best robust test quality and robust coverage can be obtained by operating the on-path latch in normal mode and all off-path latches in scan-in mode, provided that DFT circuitry and control signals allow such a combination of modes.

For example, suppose there are four latches at level-1 of Figure 1, and testing of $SCUT_0$ shows that time borrowing occurs at L_{12}, and multi-block paths that pass via L_{12} are targeted. In this case, normal mode is required at L_{12} since it is the on-path latch and a site of time borrowing. Depending on the configuration of three off-path latches, 8 ($=2^3$) configurations may be used as shown in Figure 2.



n : normal mode, s: scan-in mode, ( ): required mode for on-path latch.
An arrow from configuration A to configuration B indicates that if a path via the on-path latch is testable using configuration B, it is testable using configuration A.

Figure 2 Relationship among different latch configurations

The relationships among different configurations given by Theorems 2 and 3 are represented by arrows in Figure 2. If a path via the on-path latch (L_{12}) is robustly testable using the configuration specified by the destination of the arrow, the path is robustly testable using the configuration specified by the source of the arrow.

If a target path p is tested using a configuration where one or more off-path latches are in normal mode, then we can use the following observation to modify the value applied at the output of any latch where no time borrowing occurs and is configured in normal mode.

***Observation 1* (*Hazard-free values at non-time borrowing latches*)**: The output of a latch that does not borrow time is always hazard-free, because data stabilizes at the latch input before the latch becomes transparent. In other words, a latch that is not a site of time borrowing works like a filter of hazards rather than a buffer.

By considering both hazardous and hazard-free values at the input of this latch when a hazard-free value is desired at the output of the latch, some paths may be tested robustly that would not have been otherwise. Figure 3 shows an example case where time borrowing is detected only at L_1 but both latches are operating in normal mode to test a path via L_1. Falling transition is passed via L_1 to test the path shown in bold. Robust propagation of the falling transition at the input of G_4 requires static-1 at its off-path input, which is the output of L_2. However, the output of G_3 cannot have static-1 signal because the values at the inputs of G_3 are already determined by the on-path values as a rising and a falling transition. Hence, a conventional test generator will be unable to find a robust test for this path via L_1. On the other hand, our ATPG (automatic test pattern generator) exploits Observation 1, and considers hazardous-1 signal as well as static-1 at the input of L_2. Hence, by exploiting Observation 1, our ATPG can successfully generate a robust test for the target path and improve coverage.

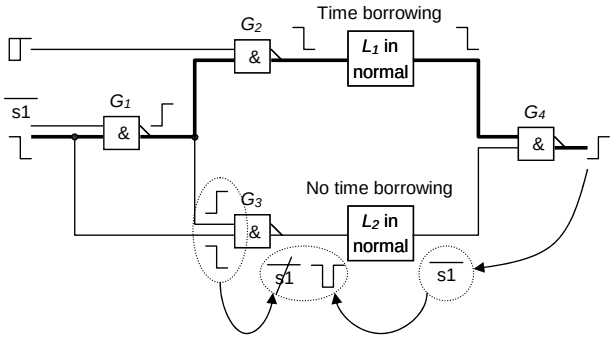


Figure 3 Hazard-free value at output of a non-time borrowing latch helps improve robust coverage

Observation 1 and above approach can be used for all cases in this paper, as long as any latch that is known not to be a site of time borrowing is configured in normal mode.

3.4 Test of paths via latches at which time borrowing does not occur

Consider a case where the objective of delay testing is to test an arbitrary multi-block path comprised of a sub-path α in C_0 and a sub-path β in C_1 in the circuit shown in Figure 1. α and β are connected by a level-1 latch L_{1i} at

which time borrowing does not occur (*i.e.*, $L_{1i} \in L^{NTB}$). Theorems 4 and 5 identify the relationship between testing α and β individually as sub-paths and testing α and β jointly (denoted as $\alpha + \beta$) as a multi-block path.

Theorem 4 (Test quality): If any robust test for α passes when C_0 is tested by itself and any robust test for β passes when C_1 is tested by itself, then the worst-case delay of multi-block path $\alpha + \beta$ via L_{1i} is within the limits imposed by the given clock period.

Proof: Given that any robust test for α passes when C_0 is tested by itself, it is guaranteed that the worst-case delay of α is such that the corresponding transition at L_{1i} will propagate to C_1 at the rising edge of the clock that drives L_{1i}. (If a robust test for α does not pass when C_0 is tested by itself, L_{1i} is known to be a site of time borrowing and thus the multi-block path $\alpha + \beta$ should be targeted in the manner described in Section 3.3.) Given that L_{1i} does not borrow time, if a robust test for the multi-block path $\alpha + \beta$ via L_{1i} fails when multi-block *SCUT* comprised of C_0 and C_1 is tested, it is evident that a robust test for β will not pass when C_1 is tested by itself. ■

Theorem 5 (Coverage): Assuming L_{1i} does not borrow time, if the multi-block path $\alpha + \beta$ is robustly testable in the multi-block *SCUT* comprised of C_0 and C_1, both α in C_0 by itself and β in C_1 by itself are individually robustly testable.

Proof: Even if the multi-block path $\alpha + \beta$ is targeted in *SCUT* comprised of C_0 and C_1, α must be robustly sensitized within C_0, as in the case where α is tested in C_0 by itself. Therefore, if α is not robustly testable in C_0 by itself, then no robust test exists for any multi-block path that includes α in C_0 and any consistent path in C_1. The same reason also applies to β. ■

In summary, if after testing blocks in transitive fan-in of a latch we conclude that time borrowing does not occur at the latch, we can test the sub-paths in the transitive fan-out of the latch instead of multi-block paths that pass via the latch.

While testing a sub-path in the fan-out of the latch L_{1i} at which no time borrowing occurs, L_{1i} may be configured either in normal mode or in scan-in mode. Section 3.4.1 explains the case where L_{1i} is configured in normal mode and Section 3.4.2 explains the case where L_{1i} is configured in scan-in mode. Again, let us consider a multi-block path via L_{1i} in Figure 1 comprised of sub-paths α and β, and assume that L_{1i} belongs to L^{NTB}.

3.4.1 Approach 1: The multi-block path of the form $\alpha + \beta$ is targeted by configuring L_{1i} in normal mode.

In this approach, the on-path latch is configured in the normal mode, *i.e.*, in a manner identical to that in Section 3.3. Hence, Theorems 1 through 3 and Corollary 1, which are related to the configuration of the off-path latches, are also applicable to Approach 1. We can further improve the test quality based on the fact that time borrowing does not occur at L_{1i}. This observation is exploited as follows.

A close-up view around L_{1i} of Figure 1 is shown in Figure 4, where P_0 represents the set of logical paths located in C_0 that are connected to the input of L_{1i}. Likewise, P_1 represents the set of logical paths that are present in C_1 in the fan-out of L_{1i}. Suppose P_0 consists of logical paths (R_0, F_0) where R_0 is the number of logical paths in C_0 that arrive at L_{1i} with a rising transition and F_0 is the number of logical paths in C_0 that arrive with a falling transition. Similarly, P_1 consists of logical paths (R_1, F_1), where R_1 is the number of logical paths that depart L_{1i} with a rising transition and F_1 is the number of logical paths that depart L_{1i} with a falling transition.

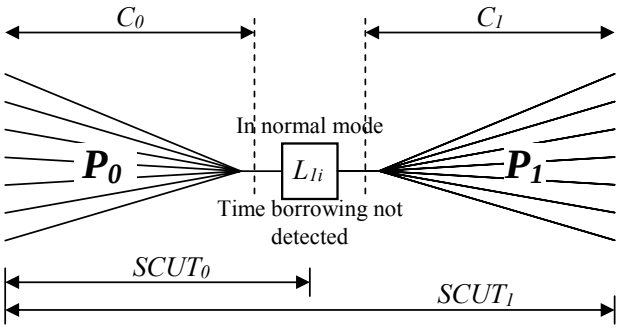


Figure 4 Use of test results for previous *SCUT*

Let P_0^* be the set of paths in P_0 that are robustly tested in $SCUT_0$ shown in Figure 4. Let π_{0+1} be the set of multi-block paths robustly tested when $SCUT_1$ (shown in Figure 4) is tested. Let P_0^{**} be the set of sub-paths of every path in π_{0+1} that completely fall within C_0. (Both P_0^* and P_0^{**} are subsets of P_0.) Then, Theorem 5 can be rephrased as $P_0^{**} \subset P_0^*$.

Based on this idea, Observation 2 describes a technique that utilizes the test results for shorter sub-paths in $SCUT_0$ to obtain higher fault coverage in combination with tests for $SCUT_1$.

Observation 2 (Use of test results for shorter sub-paths): In $SCUT_1$, instead of targeting the multi-block paths via non-time borrowing latch L_{1i}, the test generation procedure targets the paths in the transitive fan-out of the latch (P_1 region) while L_{1i} is operating in normal mode. Therefore, the sub-paths in P_0 are used only to produce a rising or a falling transition at the output of L_{1i}, and the logic values in C_0 need not robustly propagate the transition along any particular path in P_0. As long as a desired transition is initiated at the output of L_{1i}, robust propagation of the transition is required only for the sub-paths in P_1. By doing so, the number of target PDFs (path delay faults) reduces from ($R_0R_1 + F_0F_1$) to ($R_1 + F_1$).

In summary, it is shown in Theorem 5 that for P_0, testing using $SCUT_0$ provides equal or higher robust coverages compared to testing using $SCUT_1$. Also for

paths in P_1, testing using Observation 2 is superior or equal to testing multi-block paths ordinarily, since Observation 2 does not require robust sensitization along any particular path in P_0. Hence, Observation 2 shows that the robust test quality can be further improved even without using scan-in mode at the on-path latch, provided that time borrowing is known not to occur at the latch via which the target paths pass.

3.4.2 Approach 2: The sub-path β is targeted by operating L_{1i} in scan-in mode.

In this approach, we only test the sub-path β that originates at a non-time borrowing latch L_{1i}, that is configured in scan-in mode. Theorems 1 through 3 regarding the off-path latches can also be applied to Approach 2, with the difference that L_{1i} is configured in scan-in mode in Approach 2. Therefore, a statement similar to Corollary 1 can be stated for Approach 2.

Corollary 2: While testing a multi-block path via a latch at which time borrowing does not occur, the best robust test quality and robust coverage can be obtained by operating all the on-path and off-path latches in scan-in mode, provided that such a configuration is supported by the DFT hardware and control.

In this approach, the sub-path of the target that is in the fan-out of the on-path latch will be tested separately and the robust coverage for such paths will be combined with the robust coverage of the sub-paths in the fan-in of the latch.

3.5 Latch configurations required for maximum coverage

The above results provide a significant reduction in the number of latch configurations that are required to guarantee maximum robust coverage, even when time borrowing occurs at unexpected latches. In our previous approach in [1], our fully-adaptive approach required the DFT circuitry to support 2^k configurations at a level with a total of k latches. However, Figure 2 shows that when we detect time borrowing at the i^{th} latch in the level, then the configuration in which the i^{th} latch is in normal mode and all the other latches are in scan-in mode, by itself, provides the maximum coverage for all multi-block paths that pass via the i^{th} latch. Hence, no matter which and how many of the latches at the level are sites of time borrowing, maximum robust coverage can be obtained for paths that pass via latches where time borrowing occurs, if the DFT supports the following k configurations: (n, s, s, ⋯, s), (s, n, s, ⋯, s), (s, s, n, ⋯, s), ⋯ , (s, s, s, ⋯, n), where n denotes normal mode and s denotes scan-in mode. As per Corollary 2, the configuration (s, s, s, ⋯, s) provides the maximum coverage for all paths that pass via any of the latches where no time borrowing occurs. Of course, we need the configuration (n, n, n, ⋯, n) to support normal circuit operation.

Hence, if above $k+2$ configurations are supported by the DFT circuitry and control signals, then maximum possible robust coverage can be obtained. This is a significant improvement over the 2^k configurations required in our previous approach [1]. In this way, the results reduce the complexity of DFT circuitry and scan chain routing.

In summary, if there are k latches at a level, then the following configurations are sufficient to guarantee maximum robust coverage: (1) the *all-normal mode*, where all k latches are in the normal mode, (2) the *all-scan-in mode*, where all k latches are in the scan-in mode, (3) k *single-normal modes*, where only one latch along the target path is in the normal mode and all others in the scan-in mode.

The following section discusses the test generation under restrictions on latch configurations, which is a general method that encompasses the case with no restriction on latch configurations.

4. Test Generation Under Restrictions on Latch Configurations

The fully-adaptive approach described in [1] assumes that each latch may operate in any of the four modes independent of the configurations of other latches. One important advantage of this type of approach is that it can detect any unintentional time borrowing during test and adaptively modify the configurations of the latches to maximize the fault coverage. However, it is likely to suffer from high hardware and control overheads. In particular, the scan-chain design becomes very complex.

Some latch configurations may not be allowed due to considerations such as performance overheads associated with allowing scan at some latches. Also, to further reduce DFT overheads, a small number of latch configurations may be identified during circuit design based on the probability of time borrowing, p^{TB}, at each latch (the next phase of our research will precisely define p^{TB} and develop approaches to compute its value). In an extreme case where time-borrowing never occurs ($p^{TB} = 0$) at a latch, the latch need not operate in normal mode but only in scan-in mode while testing associated *SCUTs*. On the other hand, if time-borrowing at a latch is intentionally designed with a probability of time borrowing close to 1, the corresponding latch may not operate in scan-in mode while testing the corresponding *SCUTs*, unless it is desired to scan this latch to assert values at off-path lines with more ease. In this manner, presumably redundant combinations of modes may be excluded to simplify the DFT design in terms of latches, control, and scan chain routing.

The restrictions on latch configurations, however, trigger the complication of not having the optimal configuration available to test a target path under the particular time borrowing detected in a circuit under test.

In this context, we propose and demonstrate a new approach where test generation is optimized by considering time borrowing status of a circuit under test in combination with the available latch configurations. We demonstrate that this new approach exploits above observations and theorems for any available set of latch configurations to provide the corresponding maximum coverage.

4.1 Latch configuration availability

It is assumed without loss of generality that the DFT control circuit configures latches at a level collectively instead of configuring each latch independently, as was the case in the fully-adaptive approach. We assume that the more flexible the operation of a latch, the higher the overall DFT overheads. We also assume that the available configurations of latches at each level are determined prior to test generation (and definitely before any circuits are tested).

Of course, this test generation algorithm directly covers the case where all DFT configurations are available. Our approach also handles the case where some level of latches may *not* have DFT circuitry at all, if the paths within those blocks are highly delay-critical and DFT circuitry significantly aggravates the delay. In this case, only (n, n, ···, n) configuration will be available at that level. In any case as noted earlier, Observation 1 will apply if a latch at which time borrowing does not occur is operating in normal mode as an off-path latch.

4.2 Test generation strategies

One of the most important parts of the test generation under restrictions on the latch configurations is how to select the best available configuration(s) for each test session. This selection process is essentially based on Corollaries 1 and 2 and Figure 2. For the multi-block paths via a latch where time borrowing occurs, the best configuration is the single-normal mode in which only the on-path latch is in normal mode. If this single-normal mode is not feasible, a configuration should be chosen such that the on-path latch is in normal mode and as many off-path latches are in scan-in mode as possible, based on Theorems 1 through 3.

In some cases, multiple configurations may be used to target a given set of paths. For example, consider a case for the circuit in Figure 1 where multi-block paths passing via L_{12}, which is a site of time borrowing, are being targeted across level-1 latches L_{11}, L_{12}, L_{13}, and L_{14}. As shown in Figure 2, the configuration (s, n, s, s) is optimal. However, only the following configurations are supported by DFT: (n, n, n, n), (s, s, s, s), (s, n, n, n), (s, n, s, n), and (s, n, n, s). In this case, (s, s, s, s) cannot be used. Of the remaining configurations, we will use two, namely (s, n, s, n) and (s, n, n, s), since (a) both these configurations provide better coverage than (n, n, n, n) and (s, n, n, n) (See Figure 2), and (b) each one of these configurations may provide coverage for some paths that the other configuration may not cover (since there is no arrow from either of these configurations to the other in Figure 2).

We have developed an algorithm that identifies the subset of all available DFT configurations to be used for testing of any set of target paths, under any given scenario of time borrowing.

```
Procedure:ATPG_MultiSCUTs( ){
Read the pipeline circuit file and available latch configurations;
Initialize SCUT_list[level] for each level;
For each level
{
    /* select best configurations for the latches in the current level */
    For each latch of the current level {
        If(time borrowing = true & corresponding single-normal mode is available)
                Select the single-normal mode
        Else if (time borrowing = false & all-scan-in mode is available)
                Select the all-scan-in mode
        If (no config is selected above)
                Select compatible config(s)
                with the most number of latches in scan-in mode;
    }
    /* construct SCUTs */
    For each configuration selected by at least one latch {
        If (selected config consists of scan-in modes only)
                Construct an SCUT with a single stage;
                Add new SCUT to SCUT_list[level];
        Else
                Combine the selected config of current level with
                        all entries of SCUT_lilst[level – 1];
                Add new SCUT(s) to SCUT_list[level];
    }
    For all latches of all levels within the longest SCUT {
        If (time borrowing = false)
                Initialize sub-path_list[ ] for this latch to trace tested paths;
    }
    For all stage inputs within the longest SCUT {
        Initialize sub-path_list[ ] for the stage input to trace tested paths;
    }
    For each SCUT in SCUT_list[level] {
        Based on the latch configs,
                Remove/inactivate transitive fanins of latches in scan-in mode;
                Remove/inactivate transitive fanins of stage outputs except for
                        those in the last stage;
        Determine the current primary inputs and primary output;
        /* Test of an SCUT */
        Call TestATPG procedure for the current SCUT {
                For each target path {
                        Clear line values;
                        PreProcessRobust( ) {
                                Robustly sensitize the target path;
                                If (any line is removed), skip the target;
                                If (latch is met that is in normal w/o time borrowing)
                                        Target the path starting from this latch;
                        }
                        ATPGprocedure( ) {
                                Generate test for the target path;
                                Removed/inactivated parts should be ignored;
                                Implication( ) considering glitch-free signal at
                                        output of latches w/o time borrowing;
                                Write test vector to a file;
                                Accumulate PDF coverage information;
                                A path is not tested more than once;
                        }
                }
        }
    } /* end of testing all SCUTs of the current level */
    Get time borrowing results at the current output latches;
}
```

Figure 5 Proposed ATPG algorithm

In general, there may exist multiple versions of *SCUTs* in one test session (each session differs in the last stage of the target *SCUTs*) because the best latch configurations may be different for various sets of target paths. Since multiple versions of *SCUTs* are tested, it is also necessary to avoid the same path from being tested multiple times. Our proposed ATPG selects the best set of *SCUTs*, manages multiple versions of *SCUTs*, avoids any

unnecessary repetition in testing of paths, and properly computes the delay fault coverage for the entire pipeline.

The number of *SCUTs* grows especially rapidly when many combinational blocks are connected in series via latches. For example, suppose there are s versions of *SCUTs* that cover up to C_{i-1} and t configurations are selected by level-i latches. Unless a selected configuration is comprised of all-scan-in mode (all latches of a level are in the scan-in mode), each selected configuration may need to be combined with each of s *SCUTs* in the previous test session. Only if all-scan-in mode is used, the test is performed only in C_i, separately.

Our ATPG also exploits Observations 1 and 2. The ATPG algorithm is summarized in Figure 5.

4.3 Illustration of the proposed test generation approach

The proposed test generation approach is illustrated using a three-stage linear pipeline shown in Figure 6. Suppose that for level-1 latches, (L_D, L_E, L_F), DFT is designed to support three configurations: {(n, n, n), (n, s, s), (s, s, s)}, and for level-2 latches, (L_G, L_H, L_I), to support two configurations: {(n, n, n), (n, s, s)}. Note that in this example, for level-2 latches (s, s, s) configuration is not made available. In practice, this may be done, for example, to avoid performance penalty incurred along critical paths when L_G is replaced by a scan cell. In our example, this helps demonstrate how the proposed ATPG can improve the coverage even under such a restriction.

Assume time borrowing occurs at L_D, L_E, and L_I in a copy of the chip that is being tested.

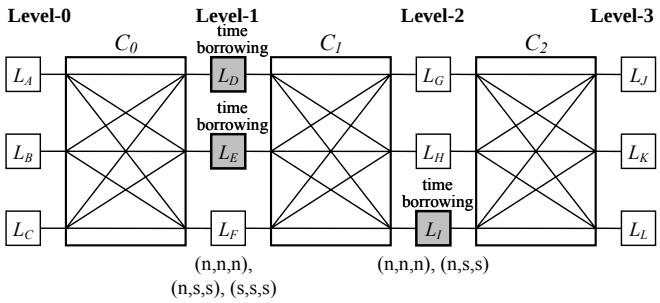


Figure 6 A three-stage linear pipeline

The *SCUTs* at each level are shown in gray in Figure 7. Bold solid lines are used to represent the paths targeted in each *SCUT*, and dotted lines are used to represent the paths that are not targeted but used as off-path. The transitive fan-ins of latches operating in scan-in mode are ignored in Figure 7, since they are not considered by the ATPG. As shown in the figure, the hazard-free property described in Observation 1 is applied to L_F, L_G, and L_H, when they are operating in normal mode but constitute off-path inputs. L_G in $SCUT_{20}$ targets sub-paths in its transitive fan-out only and the transitive fan-in is solely used to obtain desired values at the output of L_G. Observation 2 is exploited in this case by our ATPG.

The test procedure is summarized as follows. First, C_0 is tested ($SCUT_0$) and time borrowing is detected at L_D and L_E. To target the two-block paths via L_D the configuration (n, s, s) is selected at level-1 latches to obtain $SCUT_{10}$. To target the paths via L_E, (s, n, s) is desired but not available. Therefore, (n, n, n) is selected for level-1 latches to obtain $SCUT_{11}$. However, Observation 1 is exploited at the non-time borrowing off-path latch L_F. To target the sub-paths starting from L_F, (s, s, s) is selected for level-1 latches to obtain $SCUT_{12}$.

During testing of $SCUT_{10}$, $SCUT_{11}$, and $SCUT_{12}$, time borrowing is detected at L_I. For the sub-paths starting at L_G and L_H, the best configuration (s, s, s) is not available for the level-2 latches. Hence, (n, s, s) is selected instead to construct $SCUT_{20}$. Based on Observation 2, the transitive fan-in of L_G is used only to apply suitable values at L_G. Also, as a consequence, (s, s, s) is selected for the level-1 latches in $SCUT_{10}$, since for this purpose (s, s, s) at level-1 latches is superior to the other two configurations, namely (n, s, s) and (n, n, n), as per Theorems 2 and 3.

Lastly, in order to test the multi-block paths via L_I, (n, n, n) is selected for the level-2 latches when combined with each of the three *SCUTs* namely $SCUT_{10}$, $SCUT_{11}$, and $SCUT_{12}$, to give rise to $SCUT_{21}$, $SCUT_{22}$, and $SCUT_{23}$. $SCUT_{21}$ is used to test three-block paths via L_D and L_I, and $SCUT_{22}$ is used to test three-block paths via L_E and L_I. $SCUT_{23}$ is used to test two-block paths that originate at L_F and pass via L_I.

4.4 A Method to compute path delay fault coverage

In the process of testing each *SCUT*, robust path delay fault coverage is recorded at each latch located at the output of its last logic block. This record is an accumulated coverage of the paths starting from the primary inputs of the *CUT*. The record of a latch L_i consists of the number of robustly tested paths r_i arriving at the latch with a rising transition and the number of robustly tested paths f_i arriving at the latch with a falling transition, *i.e.*, (r_i, f_i). Initially, all latches in the *CUT* have (r_i, f_i) = (0, 0), and only the primary inputs have (r_i, f_i) = (1,1). Suppose the coverage of the paths arriving at a latch L_a is already recorded as (r_a, f_a) in one of the previous *SCUTs*, and time borrowing does not occur at L_a. In a following *SCUT*, if a path that starts from L_a and ends at L_b is robustly tested, (r_a, f_a) is added to (r_b, f_b) in one of the following four ways:

(1) If the transition leaving L_a and the transition arriving at L_b are both rising, r_a is added to r_b

(2) If the transition leaving L_a and the transition arriving at L_b are both falling, f_a is added to f_b

(3) If the transition leaving L_a is rising and the transition arriving at L_b is falling, r_a is added to f_b

(4) If the transition leaving L_a is falling and the transition arriving at L_b is rising, f_a is added to r_b

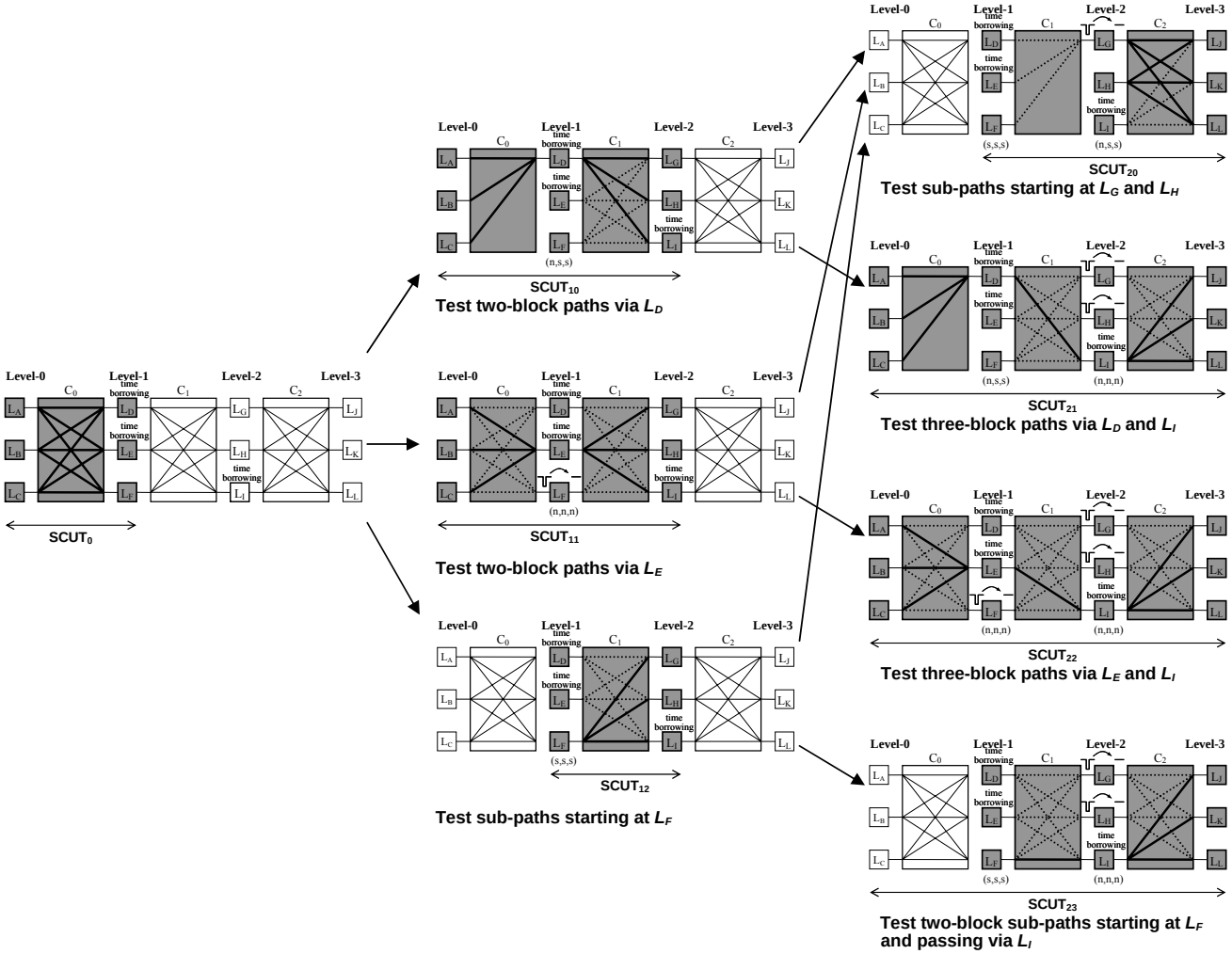


Figure 7 Test procedure – managing multiple *SCUT*s

5. Experimental Results and Comparison

We first apply the proposed approach to a ten-stage linear pipeline obtained using copies of the circuit C17 (from the ISCAS '85 benchmark suite) in the manner shown in Figure 8. The connections among ten stages are based on the two-stage pipeline comprised of two copies of C17 in [1]. Subsequently, several other circuits with various numbers of stages, namely pipelined minimum vector selectors, pipelined T1 of [3], and pipelined array multipliers, are tested, and the results are shown.

To verify the improved test quality by using the proposed method, robust PDF coverage and the number of tests are compared for four different approaches under the given latch configurations.

5.1 Test generation approaches

(1) **Classical (Classical Approach)**: The entire *CUT* is tested as a single *SCUT*, since there is no scan DFT for the latches between stages.

(2) **Previous.ext (Extended version of the approach in [1])**: The approach in [1] is modified to be applicable to the cases where not all latch configurations are available.

The new test generation method proposed in this paper is a latch-by-latch approach to construct *SCUTs* in the sense that latch configurations are determined by the considerations of each latch. In contrast, the method proposed in [1] can be regarded as a level-by-level approach in a sense that the latch configuration of each level is determined by the time borrowing status of all latches in the level collectively. Consequently, there exists a single latch configuration in each level of latches. [1] does not consider any restriction on the latch configurations, and configures the latch modes such that (a) normal mode is used for all latches that are sites of time borrowing, and (b) scan-in mode is used for latches that are not sites of time borrowing. Note that (a) is required, and (b) is not required but used to attain higher coverage. Therefore, if we impose restrictions on the latch configurations, the approach of [1] will choose a

configuration with the condition that all latches with time borrowing operate in normal mode, satisfying the condition (a). However, this selected configuration may or may not operate the non-time borrowing latches in scan-in mode depending on the available latch configurations. Hence, the extended version of the approach in [1] (Previous.ext) is implemented such that it chooses a single configuration for a level of latches that satisfies (a) and has the most number of scan-in mode for non-time borrowing latches. If there are more than one configuration that satisfies these two conditions having the same number of scan-in modes, Previous.ext selects one of them arbitrarily.

If all configurations are available or there exists a configuration that conforms to the time borrowing sites in every level of latches (*i.e.*, normal mode for every time borrowing latch and scan-in mode for every non-time borrowing latch), Previous.ext becomes the original approach in [1].

(3) **Proposed.v1 (The proposed approach without using Observation 1)**: We claim that the approach proposed in this paper improves the test quality due to three new features: (i) Improvements due to Theorems 1 through 3 (and Corollaries 1 and 2), which suggest using scan-in mode for as many off-path latches as possible. (ii) Improvements due to Observation 1 that utilizes the hazard-free property at the output of latches that are not sites of time borrowing but configured in normal mode. (iii) Improvements due to Observation 2 that targets only the sub-paths in the fan-out of a latch that is not a site of time borrowing but configured in normal mode. The first version of the proposed method, Proposed.v1, implements (i) and (iii).

(4) **Proposed.v2 (The proposed approach)**: The final version of the proposed approach, Proposed.v2, implements all three new techniques (i), (ii), and (iii).

5.2 Comparison of the four approaches

The robust PDF coverage of Previous.ext is always greater than or equal to that of classical approach regardless of what latch configurations are available.

Proposed.v1 may improve (but not reduce) test quality compared to Previous.ext if (i) Theorems 1 to 3 or (iii) Observation 2 are applicable. In Proposed.v2, the test quality can be further improved compared to Proposed.v1 if (ii) Observation 1 is applicable.

Note that the effect of each of the three new technique can be observed independently and jointly in the experiments depending on the given latch configuration and the time borrowing sites. For example, if all-scan-in mode is available, Observation 1 will never be applied since all non-time borrowing latches can operate in scan-in mode. In this case, the effect of Theorems 1 to 3 can be separately observed in the results of Proposed.v1. The effect of Observation 2 can be independently observed in Proposed.v1, for example, if all-normal mode (all latches of a level are in the normal mode) is the only available configuration in a level of latches, some of which are not sites of time borrowing (Theorems 1 to 3 is not applicable). The effect of Observation 1 can be observed independently if the test result of Proposed.v2 is superior to that of Proposed.v1.

5.3 Ten-stage pipeline using copies of C17

The ten-stage linear pipeline using copies of C17 is shown in Figure 8. We have studied seven DFT configurations and eighteen time borrowing scenarios, for each of the above four approaches. The scenarios are listed from the least frequent time borrowing (scenario (1): no time borrowing latch) to the most frequent time borrowing (scenario (18): time borrowing at every latch). The results are shown in Tables 1 to 7.

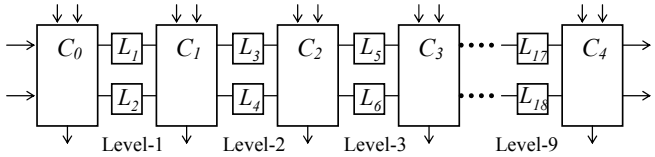


Figure 8 Ten-stage pipeline using copies of C17

The tables show the number of *SCUTs*, the number of tests, and the robust PDF coverage for each case. Note that the number of *SCUTs* and the number of tests may not directly quantify test application times, because the number of stages constituting each *SCUT* may vary depending on the configurations used and the time borrowing scenario. Hence test application time varies for each test. In the last column of the tables we specify the reasons of test quality improvement by the proposed approach compared to the test quality of Previous.ext.

In an extreme case where time borrowing does not occur, for example, scenario (1) under [DFT Config.1, 3, and 4], Previous.ext may require much higher number of tests to achieve equal or lower robust PDF coverage as the proposed approach, due to the lack of available configurations. In contrast, for the same scenario, the proposed approaches Proposed.v1 and Proposed.v2, can achieve 100% robust PDF coverage by using much smaller number of tests because of Observation 2.

In all configurations, Previous.ext obtains the same low robust PDF coverages (46.56%) as the classical approach if all latches are sites of time borrowing (scenario (18) in Tables 1 to 7), while consuming around two times the number of tests of the classical approach. In contrast, the proposed approach can improve the coverage in most cases, in some cases significantly, *e.g.*, [DFT Config.4, 6, and 7].

In particular, as mentioned earlier, Table 7 [DFT Config.7] is the case where the original approach in [1] can be applied without modification. As the results show, if time borrowing does not occur at many sites (scenario

(1) to (7) in Table 7), the robust PDF coverages for Previous.ext and Proposed.v1 (and Proposed.v2) are identical. In contrast, if time borrowing occurs extensively such as the scenarios 8 to 18, the proposed approaches (Proposed.v1 and Proposed.v2) can improve the coverage significantly to 100%, whereas Previous.ext can achieve the coverages around 50%.

There exist 30,574 target PDFs in this ten-stage pipeline of C17. Therefore, even if the classical approach can test all PDFs robustly, it needs 30,574 tests in the worst case, and most tests are multi-block paths that pass via ten stages requiring long test application time. On the other hand, the proposed approach, in majority of cases, takes advantage of scan DFT to reduce the number of tests while enhancing the robust PDF coverage. In the worst case among the experiments, the proposed approach requires as many as 40,740 or 60,460 tests to achieve 100% coverage, which indicates the trade-off between the robust coverage and test application time. However, not all of these tests require propagating through ten stages. Hence, the actual test application time on average will be less than that of the classical approach assuming the classical approach is able to achieve 100% coverage.

With regard to the effect of pipeline length (the number of stages) on the test quality, the results for the ten-stage pipeline using C17 in Tables 1 to 7 and the results for two- and five-stage pipelines using C17 illustrate that as the number of stages increases, the coverage decreases for the classical approach and Previous.ext, while the coverage for the proposed approach does not decrease significantly. This shows that the proposed approach becomes more efficient in testing pipelines with more stages compared to the classical and Previous.ext approaches.

More results for pipelines using copies of T1 of [3] and pipelines of array multiplier are presented in Tables 8 to 16.

Table 1 Ten-stage C17 pipeline: [DFT Config.1] (n,n) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from Previous.ext
(1) None	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	220	100.00	Obs2
	Proposed.v2	10	220	100.00	Obs2
(2) L_3, L_{10}, L_{11}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	272	98.46	Obs2
	Proposed.v2	10	276	98.96	Obs1, Obs2
(3) L_4, L_{12}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	319	74.36	Obs2
	Proposed.v2	10	325	83.77	Obs1, Obs2
(4) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	490	91.73	Obs2
	Proposed.v2	10	490	91.73	Obs2
(5) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	25671	50.71	Obs2
	Proposed.v2	10	29402	62.92	Obs1, Obs2
(6) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	410	83.54	Obs2
	Proposed.v2	10	426	88.99	Obs1, Obs2
(7) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	435	71.00	Obs2
	Proposed.v2	10	453	82.02	Obs1, Obs2
(8) L_1, L_3, L_6, L_7, L_8, L_9, L_{10}, L_{11}, L_{14}, L_{15}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	974	55.46	Obs2
	Proposed.v2	10	1009	62.86	Obs1, Obs2
(9) All but L_1, L_2	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	14549	46.67	Obs2
	Proposed.v2	10	14549	46.67	Obs2
(10) All but L_3, L_4	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	7438	46.92	Obs2
	Proposed.v2	10	7438	46.92	Obs2
(11) All but L_5, L_6	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	3938	47.41	Obs2
	Proposed.v2	10	3638	47.41	Obs2
(12) All but L_7, L_8	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	2344	48.29	Obs2
	Proposed.v2	10	2344	48.29	Obs2
(13) All but L_9, L_{10}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	1886	49.81	Obs2
	Proposed.v2	10	1886	49.81	Obs2
(14) All but L_{11}, L_{12}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	2344	52.32	Obs2
	Proposed.v2	10	2344	52.32	Obs2
(15) All but L_{13}, L_{14}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	3938	56.28	Obs2
	Proposed.v2	10	3938	56.28	Obs2
(16) All but L_{15}, L_{16}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	7438	62.08	Obs2
	Proposed.v2	10	7438	62.08	Obs2
(17) All but L_{17}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	14549	73.65	Obs2
	Proposed.v2	10	14549	73.65	Obs2
(18) All latches L_1 to L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	28763	46.56	Obs2
	Proposed.v2	10	28763	46.56	Obs2

Table 2 Ten-stage C17 pipeline:
[DFT Config.2] (n,n), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	14236	46.56	
	Previous.ext	10	220	100.00	
	Proposed.v1	10	220	100.00	-
	Proposed.v2	10	220	100.00	-
(2) L_3, L_{10}, L_{11}	Classical	1	14236	46.56	
	Previous.ext	10	398	95.28	
	Proposed.v1	14	272	98.46	Thm1-3
	Proposed.v2	14	276	98.96	Thm1-3, Obs1
(3) L_4, L_{12}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	435	59.23	
	Proposed.v1	15	319	74.36	Thm1-3
	Proposed.v2	15	325	83.77	Thm1-3, Obs1
(4) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	55	490	91.73	Thm1-3
	Proposed.v2	55	490	91.73	Thm1-3
(5) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	35	25671	50.71	Thm1-3
	Proposed.v2	35	29402	62.92	Thm1-3, Obs1
(6) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	27	410	83.54	Thm1-3
	Proposed.v2	27	426	88.99	Thm1-3, Obs1
(7) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	27	435	71.00	Thm1-3
	Proposed.v2	27	453	82.02	Thm1-3, Obs1
(8) L_1, L_3, L_6, L_7, L_8, L_9, L_{10}, L_{11}, L_{14}, L_{15}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	26	974	55.46	Thm1-3
	Proposed.v2	26	1009	62.86	Thm1-3, Obs1
(9) All but L_1, L_2	Classical	1	14236	46.56	
	Previous.ext	10	14549	46.67	
	Proposed.v1	10	14549	46.67	-
	Proposed.v2	10	14549	46.67	-
(10) All but L_3, L_4	Classical	1	14236	46.56	
	Previous.ext	10	7438	46.92	
	Proposed.v1	10	7438	46.92	-
	Proposed.v2	10	7438	46.92	-
(11) All but L_5, L_6	Classical	1	14236	46.56	
	Previous.ext	10	3938	47.41	
	Proposed.v1	10	3938	47.41	-
	Proposed.v2	10	3938	47.41	-
(12) All but L_7, L_8	Classical	1	14236	46.56	
	Previous.ext	10	2344	48.29	
	Proposed.v1	10	2344	48.29	-
	Proposed.v2	10	2344	48.29	-
(13) All but L_9, L_{10}	Classical	1	14236	46.56	
	Previous.ext	10	1886	49.81	
	Proposed.v1	10	1886	49.81	-
	Proposed.v2	10	1886	49.81	-
(14) All but L_{11}, L_{12}	Classical	1	14236	46.56	
	Previous.ext	10	2344	52.32	
	Proposed.v1	10	2344	52.32	-
	Proposed.v2	10	2344	52.32	-
(15) All but L_{13}, L_{14}	Classical	1	14236	46.56	
	Previous.ext	10	3938	56.28	
	Proposed.v1	10	3938	56.28	-
	Proposed.v2	10	3938	56.28	-
(16) All but L_{15}, L_{16}	Classical	1	14236	46.56	
	Previous.ext	10	7438	62.08	
	Proposed.v1	10	7438	62.08	-
	Proposed.v2	10	7438	62.08	-
(17) All but L_{17}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	14549	73.65	
	Proposed.v1	10	14549	73.65	-
	Proposed.v2	10	14549	73.65	-
(18) All latches L_1 to L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	10	28763	46.56	-
	Proposed.v2	10	28763	46.56	-

Table 3 Ten-stage C17 pipeline:
[DFT Config.3] (n,n), (n,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	14236	46.56	
	Previous.ext	10	580	100.00	
	Proposed.v1	10	220	100.00	Obs2
	Proposed.v2	10	220	100.00	Obs2
(2) L_3, L_{10}, L_{11}	Classical	1	14236	46.56	
	Previous.ext	10	645	98.49	
	Proposed.v1	12	278	98.74	Thm1-3, Obs2
	Proposed.v2	12	282	99.24	Thm1-3, Obs1&2
(3) L_4, L_{12}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	757	71.73	
	Proposed.v1	13	321	76.44	Thm1-3, Obs2
	Proposed.v2	13	327	85.85	Thm1-3, Obs1&2
(4) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	580	100.00	
	Proposed.v1	10	580	100.00	-
	Proposed.v2	10	580	100.00	-
(5) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	35	25671	50.71	Thm1-3, Obs2
	Proposed.v2	35	29402	62.92	Thm1-3, Obs1&2
(6) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	840	83.57	
	Proposed.v1	18	428	86.31	Thm1-3, Obs2
	Proposed.v2	18	444	91.76	Thm1-3, Obs1&2
(7) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	905	66.85	
	Proposed.v1	19	451	72.38	Thm1-3, Obs2
	Proposed.v2	19	469	83.40	Thm1-3, Obs1&2
(8) L_1, L_3, L_6, L_7, L_8, L_9, L_{10}, L_{11}, L_{14}, L_{15}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	1478	52.57	
	Proposed.v1	27	1033	56.98	Thm1-3, Obs2
	Proposed.v2	27	1068	64.38	Thm1-3, Obs1&2
(9) All but L_1, L_2	Classical	1	14236	46.56	
	Previous.ext	10	14621	46.67	
	Proposed.v1	86	15772	50.82	Thm1-3, Obs2
	Proposed.v2	86	15772	50.82	Thm1-3, Obs2
(10) All but L_3, L_4	Classical	1	14236	46.56	
	Previous.ext	10	7638	46.92	
	Proposed.v1	67	8033	51.09	Thm1-3, Obs2
	Proposed.v2	67	8033	51.09	Thm1-3, Obs2
(11) All but L_5, L_6	Classical	1	14236	46.56	
	Previous.ext	10	4302	47.41	
	Proposed.v1	50	4228	51.59	Thm1-3, Obs2
	Proposed.v2	50	4228	51.59	Thm1-3, Obs2
(12) All but L_7, L_8	Classical	1	14236	46.56	
	Previous.ext	10	2920	48.29	
	Proposed.v1	43	2497	52.51	Thm1-3, Obs2
	Proposed.v2	43	2497	52.51	Thm1-3, Obs2
(13) All but L_9, L_{10}	Classical	1	14236	46.56	
	Previous.ext	10	2746	49.81	
	Proposed.v1	38	2000	54.09	Thm1-3, Obs2
	Proposed.v2	38	2000	54.09	Thm1-3, Obs2
(14) All but L_{11}, L_{12}	Classical	1	14236	46.56	
	Previous.ext	10	3584	52.32	
	Proposed.v1	43	2497	56.72	Thm1-3, Obs2
	Proposed.v2	43	2497	56.72	Thm1-3, Obs2
(15) All but L_{13}, L_{14}	Classical	1	14236	46.56	
	Previous.ext	10	5648	56.28	
	Proposed.v1	50	4228	60.95	Thm1-3, Obs2
	Proposed.v2	50	4228	60.95	Thm1-3, Obs2
(16) All but L_{15}, L_{16}	Classical	1	14236	46.56	
	Previous.ext	10	9582	62.08	
	Proposed.v1	67	8033	67.28	Thm1-3, Obs2
	Proposed.v2	67	8033	67.28	Thm1-3, Obs2
(17) All but L_{17}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	16605	73.65	
	Proposed.v1	86	15772	75.71	Thm1-3, Obs2
	Proposed.v2	86	15772	75.71	Thm1-3, Obs2
(18) All latches L_1 to L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	115	31255	50.71	Thm1-3, Obs2
	Proposed.v2	115	31255	50.71	Thm1-3, Obs2

Table 4 Ten-stage C17 pipeline:
[DFT Config.4] (n,n), (s,n) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	14236	46.56	
	Previous.ext	10	40740	100.00	
	Proposed.v1	10	220	100.00	Obs2
	Proposed.v2	10	220	100.00	Obs2
(2) L_3, L_{10}, L_{11}	Classical	1	14236	46.56	
	Previous.ext	10	40414	96.79	
	Proposed.v1	12	287	99.46	Thm1-3, Obs2
	Proposed.v2	12	287	99.46	Thm1-3, Obs2
(3) L_4, L_{12}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	39467	87.50	
	Proposed.v1	12	346	97.92	Thm1-3, Obs2
	Proposed.v2	12	346	97.92	Thm1-3, Obs2
(4) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	55	490	91.73	Thm1-3, Obs2
	Proposed.v2	55	490	91.73	Thm1-3, Obs2
(5) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	40740	100.00	
	Proposed.v1	10	40740	100.00	-
	Proposed.v2	10	40740	100.00	-
(6) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	37365	66.85	
	Proposed.v1	19	470	94.47	Thm1-3, Obs2
	Proposed.v2	19	470	94.47	Thm1-3, Obs2
(7) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	39068	83.57	
	Proposed.v1	18	504	97.26	Thm1-3, Obs2
	Proposed.v2	18	504	97.26	Thm1-3, Obs2
(8) L_1, L_3, L_6, L_7, L_8, L_9, L_{10}, L_{11}, L_{14}, L_{15}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	38572	81.90	
	Proposed.v1	28	1415	97.00	Thm1-3, Obs2
	Proposed.v2	28	1415	97.00	Thm1-3, Obs2
(9) All but L_1, L_2	Classical	1	14236	46.56	
	Previous.ext	10	28874	46.67	
	Proposed.v1	90	27506	91.74	Thm1-3, Obs2
	Proposed.v2	90	27506	91.74	Thm1-3, Obs2
(10) All but L_3, L_4	Classical	1	14236	46.56	
	Previous.ext	10	29143	46.92	
	Proposed.v1	67	13599	91.75	Thm1-3, Obs2
	Proposed.v2	67	13599	91.75	Thm1-3, Obs2
(11) All but L_5, L_6	Classical	1	14236	46.56	
	Previous.ext	10	29628	47.41	
	Proposed.v1	54	6824	91.79	Thm1-3, Obs2
	Proposed.v2	54	6824	91.79	Thm1-3, Obs2
(12) All but L_7, L_8	Classical	1	14236	46.56	
	Previous.ext	10	30394	48.29	
	Proposed.v1	43	3771	91.85	Thm1-3, Obs2
	Proposed.v2	43	3771	91.85	Thm1-3, Obs2
(13) All but L_9, L_{10}	Classical	1	14236	46.56	
	Previous.ext	10	31491	49.81	
	Proposed.v1	42	2900	91.98	Thm1-3, Obs2
	Proposed.v2	42	2900	91.98	Thm1-3, Obs2
(14) All but L_{11}, L_{12}	Classical	1	14236	46.56	
	Previous.ext	10	32899	52.32	
	Proposed.v1	43	3771	92.25	Thm1-3, Obs2
	Proposed.v2	43	3771	92.25	Thm1-3, Obs2
(15) All but L_{13}, L_{14}	Classical	1	14236	46.56	
	Previous.ext	10	34418	56.28	
	Proposed.v1	54	6824	92.77	Thm1-3, Obs2
	Proposed.v2	54	6824	92.77	Thm1-3, Obs2
(16) All but L_{15}, L_{16}	Classical	1	14236	46.56	
	Previous.ext	10	35488	62.08	
	Proposed.v1	67	13599	93.82	Thm1-3, Obs2
	Proposed.v2	67	13599	93.82	Thm1-3, Obs2
(17) All but L_{17}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	34989	73.65	
	Proposed.v1	90	27506	95.91	Thm1-3, Obs2
	Proposed.v2	90	27506	95.91	Thm1-3, Obs2
(18) All latches L_1 to L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	115	55530	91.73	Thm1-3, Obs2
	Proposed.v2	115	55530	91.73	Thm1-3, Obs2

Table 5 Ten-stage C17 pipeline:
[DFT Config.5] (n,n), (n,s), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	14236	46.56	
	Previous.ext	10	220	100.00	
	Proposed.v1	10	220	100.00	-
	Proposed.v2	10	220	100.00	-
(2) L_3, L_{10}, L_{11}	Classical	1	14236	46.56	
	Previous.ext	10	290	98.49	
	Proposed.v1	14	278	98.74	Thm1-3
	Proposed.v2	14	282	99.24	Thm1-3, Obs1
(3) L_4, L_{12}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	347	71.73	
	Proposed.v1	14	321	76.44	Thm1-3
	Proposed.v2	14	327	85.85	Thm1-3, Obs1
(4) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	580	100.00	
	Proposed.v1	35	580	100.00	-
	Proposed.v2	35	580	100.00	-
(5) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	35	25671	50.71	Thm1-3
	Proposed.v2	35	29402	62.92	Thm1-3, Obs1
(6) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	840	83.57	
	Proposed.v1	23	428	86.31	Thm1-3
	Proposed.v2	23	444	91.76	Thm1-3, Obs1
(7) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	905	66.85	
	Proposed.v1	23	451	72.38	Thm1-3
	Proposed.v2	23	469	83.40	Thm1-3, Obs1
(8) L_1, L_3, L_6, L_7, L_8, L_9, L_{10}, L_{11}, L_{14}, L_{15}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	1478	52.57	
	Proposed.v1	30	1033	56.98	Thm1-3
	Proposed.v2	30	1068	64.38	Thm1-3, Obs1
(9) All but L_1, L_2	Classical	1	14236	46.56	
	Previous.ext	10	14549	46.67	
	Proposed.v1	86	15772	50.82	Thm1-3
	Proposed.v2	86	15772	50.82	Thm1-3
(10) All but L_3, L_4	Classical	1	14236	46.56	
	Previous.ext	10	7438	46.92	
	Proposed.v1	67	8033	51.09	Thm1-3
	Proposed.v2	67	8033	51.09	Thm1-3
(11) All but L_5, L_6	Classical	1	14236	46.56	
	Previous.ext	10	3938	47.41	
	Proposed.v1	50	4228	51.59	Thm1-3
	Proposed.v2	50	4228	51.59	Thm1-3
(12) All but L_7, L_8	Classical	1	14236	46.56	
	Previous.ext	10	2344	48.29	
	Proposed.v1	43	2497	52.51	Thm1-3
	Proposed.v2	43	2497	52.51	Thm1-3
(13) All but L_9, L_{10}	Classical	1	14236	46.56	
	Previous.ext	10	1886	49.81	
	Proposed.v1	38	2000	54.09	Thm1-3
	Proposed.v2	38	2000	54.09	Thm1-3
(14) All but L_{11}, L_{12}	Classical	1	14236	46.56	
	Previous.ext	10	2344	52.32	
	Proposed.v1	43	2497	56.72	Thm1-3
	Proposed.v2	43	2497	56.72	Thm1-3
(15) All but L_{13}, L_{14}	Classical	1	14236	46.56	
	Previous.ext	10	3938	56.28	
	Proposed.v1	50	4228	60.95	Thm1-3
	Proposed.v2	50	4228	60.95	Thm1-3
(16) All but L_{15}, L_{16}	Classical	1	14236	46.56	
	Previous.ext	10	7438	62.08	
	Proposed.v1	67	8033	67.28	Thm1-3
	Proposed.v2	67	8033	67.28	Thm1-3
(17) All but L_{17}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	14549	73.65	
	Proposed.v1	86	15772	75.71	Thm1-3
	Proposed.v2	86	15772	75.71	Thm1-3
(18) All latches L_1 to L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	115	31255	50.71	Thm1-3
	Proposed.v2	115	31255	50.71	Thm1-3

Table 6 Ten-stage C17 pipeline:
[DFT Config.6] (n,n), (s,n), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	14236	46.56	
	Previous.ext	10	220	100.00	
	Proposed.v1	10	220	100.00	-
	Proposed.v2	10	220	100.00	-
(2) L_3, L_{10}, L_{11}	Classical	1	14236	46.56	
	Previous.ext	10	404	96.79	
	Proposed.v1	13	287	99.46	Thm1-3
	Proposed.v2	13	287	99.46	Thm1-3
(3) L_4, L_{12}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	457	87.50	
	Proposed.v1	15	346	97.92	Thm1-3
	Proposed.v2	15	346	97.92	Thm1-3
(4) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	55	490	91.73	Thm1-3
	Proposed.v2	23	490	91.73	Thm1-3
(5) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	40740	100.00	
	Proposed.v1	35	40740	100.00	-
	Proposed.v2	35	40740	100.00	-
(6) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	37365	66.85	
	Proposed.v1	23	470	94.47	Thm1-3
	Proposed.v2	23	470	94.47	Thm1-3
(7) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	39068	83.57	
	Proposed.v1	23	504	97.26	Thm1-3
	Proposed.v2	23	504	97.26	Thm1-3
(8) L_1, L_3, L_6, L_7, L_8, L_9, L_{10}, L_{11}, L_{14}, L_{15}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	38572	81.90	
	Proposed.v1	35	1415	97.00	Thm1-3
	Proposed.v2	35	1415	97.00	Thm1-3
(9) All but L_1, L_2	Classical	1	14236	46.56	
	Previous.ext	10	14549	46.67	
	Proposed.v1	90	27506	91.74	Thm1-3
	Proposed.v2	90	27506	91.74	Thm1-3
(10) All but L_3, L_4	Classical	1	14236	46.56	
	Previous.ext	10	7438	46.92	
	Proposed.v1	67	13599	91.75	Thm1-3
	Proposed.v2	67	13599	91.75	Thm1-3
(11) All but L_5, L_6	Classical	1	14236	46.56	
	Previous.ext	10	3938	47.41	
	Proposed.v1	54	6824	91.79	Thm1-3
	Proposed.v2	54	6824	91.79	Thm1-3
(12) All but L_7, L_8	Classical	1	14236	46.56	
	Previous.ext	10	2344	48.29	
	Proposed.v1	43	3771	91.85	Thm1-3
	Proposed.v2	43	3771	91.85	Thm1-3
(13) All but L_9, L_{10}	Classical	1	14236	46.56	
	Previous.ext	10	1886	49.81	
	Proposed.v1	42	2900	91.98	Thm1-3
	Proposed.v2	42	2900	91.98	Thm1-3
(14) All but L_{11}, L_{12}	Classical	1	14236	46.56	
	Previous.ext	10	2344	52.32	
	Proposed.v1	43	3771	92.25	Thm1-3
	Proposed.v2	43	3771	92.25	Thm1-3
(15) All but L_{13}, L_{14}	Classical	1	14236	46.56	
	Previous.ext	10	3938	56.28	
	Proposed.v1	54	6824	92.77	Thm1-3
	Proposed.v2	54	6824	92.77	Thm1-3
(16) All but L_{15}, L_{16}	Classical	1	14236	46.56	
	Previous.ext	10	7438	62.08	
	Proposed.v1	67	13599	93.82	Thm1-3
	Proposed.v2	67	13599	93.82	Thm1-3
(17) All but L_{17}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	14549	73.65	
	Proposed.v1	90	27506	95.91	Thm1-3
	Proposed.v2	90	27506	95.91	Thm1-3
(18) All latches L_1 to L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	115	55530	91.73	Thm1-3
	Proposed.v2	115	55530	91.73	Thm1-3

Table 7 Ten-stage C17 pipeline:
[DFT Config.7] (n,n), (n,s), (s,n), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	14236	46.56	
	Previous.ext	10	220	100.00	
	Proposed.v1	10	220	100.00	-
	Proposed.v2	10	220	100.00	-
(2) L_3, L_{10}, L_{11}	Classical	1	14236	46.56	
	Previous.ext	10	296	100.00	
	Proposed.v1	13	296	100.00	-
	Proposed.v2	13	296	100.00	-
(3) L_4, L_{12}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	348	100.00	
	Proposed.v1	14	348	100.00	-
	Proposed.v2	14	348	100.00	-
(4) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	580	100.00	
	Proposed.v1	35	580	100.00	-
	Proposed.v2	35	580	100.00	-
(5) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	40740	100.00	
	Proposed.v1	35	40740	100.00	-
	Proposed.v2	35	40740	100.00	-
(6) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	14236	46.56	
	Previous.ext	10	500	100.00	
	Proposed.v1	19	500	100.00	-
	Proposed.v2	19	500	100.00	-
(7) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	532	100.00	
	Proposed.v1	19	532	100.00	-
	Proposed.v2	19	532	100.00	-
(8) L_1, L_3, L_6, L_7, L_8, L_9, L_{10}, L_{11}, L_{14}, L_{15}, L_{16}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	1154	85.27	
	Proposed.v1	28	1520	100.00	Thm1-3
	Proposed.v2	28	1520	100.00	Thm1-3
(9) All but L_1, L_2	Classical	1	14236	46.56	
	Previous.ext	10	14549	46.67	
	Proposed.v1	90	29908	100.00	Thm1-3
	Proposed.v2	90	29908	100.00	Thm1-3
(10) All but L_3, L_4	Classical	1	14236	46.56	
	Previous.ext	10	7438	46.92	
	Proposed.v1	67	14752	100.00	Thm1-3
	Proposed.v2	67	14752	100.00	Thm1-3
(11) All but L_5, L_6	Classical	1	14236	46.56	
	Previous.ext	10	3938	47.41	
	Proposed.v1	54	7372	100.00	Thm1-3
	Proposed.v2	54	7372	100.00	Thm1-3
(12) All but L_7, L_8	Classical	1	14236	46.56	
	Previous.ext	10	2344	48.29	
	Proposed.v1	43	4048	100.00	Thm1-3
	Proposed.v2	43	4048	100.00	Thm1-3
(13) All but L_9, L_{10}	Classical	1	14236	46.56	
	Previous.ext	10	1886	49.81	
	Proposed.v1	42	3100	100.00	Thm1-3
	Proposed.v2	42	3100	100.00	Thm1-3
(14) All but L_{11}, L_{12}	Classical	1	14236	46.56	
	Previous.ext	10	2344	52.32	
	Proposed.v1	43	4048	100.00	Thm1-3
	Proposed.v2	43	4048	100.00	Thm1-3
(15) All but L_{13}, L_{14}	Classical	1	14236	46.56	
	Previous.ext	10	3938	56.28	
	Proposed.v1	54	7372	100.00	Thm1-3
	Proposed.v2	54	7372	100.00	Thm1-3
(16) All but L_{15}, L_{16}	Classical	1	14236	46.56	
	Previous.ext	10	7438	62.08	
	Proposed.v1	67	14752	100.00	Thm1-3
	Proposed.v2	67	14752	100.00	Thm1-3
(17) All but L_{17}, L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	14549	73.65	
	Proposed.v1	90	29908	100.00	Thm1-3
	Proposed.v2	90	29908	100.00	Thm1-3
(18) All latches L_1 to L_{18}	Classical	1	14236	46.56	
	Previous.ext	10	28763	46.56	
	Proposed.v1	115	60460	100.00	Thm1-3
	Proposed.v2	115	60460	100.00	Thm1-3

Table 8 Five-stage T1 pipeline:
[DFT Config] (n,n), (n,s) at level-1 through level-4

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	380	28.70	
	Previous.ext	5	890	100	
	Proposed.v1	5	110	100	Obs2
	Proposed.v2	5	110	100	Obs2
(2) L_1, L_6	Classical	1	380	28.70	
	Previous.ext	5	780	56.95	
	Proposed.v1	6	148	86.40	Thm1-3, Obs2
	Proposed.v2	6	148	86.40	Thm1-3, Obs2
(3) L_1, L_2	Classical	1	380	28.70	
	Previous.ext	5	798	69.18	
	Proposed.v1	6	148	89.73	Thm1-3, Obs2
	Proposed.v2	6	148	89.73	Thm1-3, Obs2
(4) L_1, L_4, L_5, L_8	Classical	1	380	28.70	
	Previous.ext	5	656	40.79	
	Proposed.v1	9	251	76.66	Thm1-3, Obs2
	Proposed.v2	9	251	76.66	Thm1-3, Obs2
(5) L_1, L_2, L_5, L_6	Classical	1	380	28.70	
	Previous.ext	5	698	47.28	
	Proposed.v1	7	186	79.15	Thm1-3, Obs2
	Proposed.v2	7	186	79.15	Thm1-3, Obs2
(6) All latches L_1 to L_8	Classical	1	380	28.70	
	Previous.ext	5	726	28.70	
	Proposed.v1	31	1497	67.82	Thm1-3, Obs2
	Proposed.v2	31	1497	67.82	Thm1-3, Obs2

Table 9 Five-stage pipeline of array multiplier:
[DFT Config.] all-normal and all-scan-in modes in all levels

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	640	9.54	
	Previous.ext	5	478	100	
	Proposed.v1	5	478	100	-
	Proposed.v2	5	478	100	-
(2) L_{12}, L_{14}, L_{34}, L_{36}, L_{37}	Classical	1	640	9.54	
	Previous.ext	5	902	95.35	
	Proposed.v1	7	764	96.66	Thm1-3
	Proposed.v2	7	764	96.66	Thm1-3
(3) L_{10}, L_{14}, L_{24}, L_{28}, L_{33}, L_{39}, L_{44}	Classical	1	640	9.54	
	Previous.ext	5	1459	9.54	
	Proposed.v1	13	755	82.40	Thm1-3
	Proposed.v2	13	782	85.16	Thm1-3, Obs1
(4) L_{21}, L_{24}, L_{27}, L_{31}, L_{33}, L_{36}, L_{42}, L_{44}	Classical	1	640	9.54	
	Previous.ext	5	2158	18.65	
	Proposed.v1	11	1174	61.74	Thm1-3
	Proposed.v2	11	1280	63.13	Thm1-3, Obs1
(5) L_{14}, L_{15}, L_{21}, L_{22}, L_{27}, L_{29}, L_{30}, L_{33}, L_{37}, L_{44}	Classical	1	640	9.54	
	Previous.ext	5	1459	9.54	
	Proposed.v1	13	855	77.36	Thm1-3
	Proposed.v2	13	858	77.68	Thm1-3, Obs1
(6) All latches L_1 to L_{18}	Classical	1	640	9.54	
	Previous.ext	5	1459	9.54	
	Proposed.v1	5	1459	9.54	-
	Proposed.v2	5	1459	9.54	-

Table 10 Ten-stage T1 pipeline:
[DFT Config.1] (n,n) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	184	50.10	Thm1-3, Obs2
	Proposed.v2	10	184	50.10	Thm1-3, Obs2
(2) L_3, L_{10}, L_{11}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	236	36.72	Thm1-3, Obs2
	Proposed.v2	10	236	36.72	Thm1-3, Obs2
(3) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	1402	7.59	Thm1-3, Obs2
	Proposed.v2	10	1402	7.59	Thm1-3, Obs2
(4) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	544	50.02	Thm1-3, Obs2
	Proposed.v2	10	544	50.02	Thm1-3, Obs2
(5) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	666	22.48	Thm1-3, Obs2
	Proposed.v2	10	666	22.48	Thm1-3, Obs2
(6) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	640	25.08	Thm1-3, Obs2
	Proposed.v2	10	640	25.08	Thm1-3, Obs2
(7) All but L_9, L_{10}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	1826	10.80	Thm1-3, Obs2
	Proposed.v2	10	1826	10.80	Thm1-3, Obs2
(8) All latches L_1 to L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	24514	7.51	-
	Proposed.v2	10	24514	7.51	-

Table 11 Ten-stage T1 pipeline:
[DFT Config.2] (n,n), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	12284	7.51	
	Previous.ext	10	220	100	
	Proposed.v1	10	220	100	-
	Proposed.v2	10	220	100	-
(2) L_3, L_{10}, L_{11}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	14	272	48.42	Thm1-3
	Proposed.v2	14	272	48.42	Thm1-3
(3) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	1456	7.62	Thm1-3
	Proposed.v2	55	1456	7.62	Thm1-3
(4) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	580	54.69	Thm1-3
	Proposed.v2	55	580	54.69	Thm1-3
(5) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	700	23.73	Thm1-3
	Proposed.v2	55	700	23.73	Thm1-3
(6) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	676	26.76	Thm1-3
	Proposed.v2	55	676	26.76	Thm1-3
(7) All but L_9, L_{10}	Classical	1	12284	7.51	
	Previous.ext	10	1452	10.65	
	Proposed.v1	10	1836	10.81	Thm1-3
	Proposed.v2	10	1836	10.81	Thm1-3
(8) All latches L_1 to L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	10	24514	7.51	-
	Proposed.v2	10	24514	7.51	-

Table 12 Ten-stage T1 pipeline:
[DFT Config.3] (n,n), (n,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	12284	7.51	
	Previous.ext	10	30610	100	
	Proposed.v1	10	220	100	Thm1-3, Obs2
	Proposed.v2	10	220	100	Thm1-3, Obs2
(2) L_3, L_{10}, L_{11}	Classical	1	12284	7.51	
	Previous.ext	10	350	55.60	
	Proposed.v1	12	300	86.23	Thm1-3, Obs2
	Proposed.v2	12	300	86.23	Thm1-3, Obs2
(3) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	30610	100	
	Proposed.v1	10	30610	100	-
	Proposed.v2	10	30610	100	-
(4) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	580	54.69	Thm1-3, Obs2
	Proposed.v2	55	580	54.69	Thm1-3, Obs2
(5) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	18352	25.51	
	Proposed.v1	30	820	64.52	Thm1-3, Obs2
	Proposed.v2	30	820	64.52	Thm1-3, Obs2
(6) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	19514	22.62	
	Proposed.v1	35	770	61.17	Thm1-3, Obs2
	Proposed.v2	35	770	61.17	Thm1-3, Obs2
(7) All but L_9, L_{10}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	78	4310	55.86	Thm1-3, Obs2
	Proposed.v2	78	4310	55.86	Thm1-3, Obs2
(8) All latches L_1 to L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	1023	147605	54.69	Thm1-3, Obs2
	Proposed.v2	1023	147605	54.69	Thm1-3, Obs2

Table 13 Ten-stage T1 pipeline:
[DFT Config.4] (n,n), (s,n) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	12284	7.51	
	Previous.ext	10	940	100	
	Proposed.v1	10	220	100	Thm1-3, Obs2
	Proposed.v2	10	220	100	Thm1-3, Obs2
(2) L_3, L_{10}, L_{11}	Classical	1	12284	7.51	
	Previous.ext	10	304	41.37	
	Proposed.v1	12	284	53.56	Thm1-3, Obs2
	Proposed.v2	12	284	53.56	Thm1-3, Obs2
(3) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	1456	7.62	Thm1-3, Obs2
	Proposed.v2	55	1456	7.62	Thm1-3, Obs2
(4) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	940	100	
	Proposed.v1	10	940	100	-
	Proposed.v2	10	940	100	-
(5) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	2538	22.62	
	Proposed.v1	35	736	25.61	Thm1-3, Obs2
	Proposed.v2	35	736	25.61	Thm1-3, Obs2
(6) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	2174	25.51	
	Proposed.v1	30	721	30.13	Thm1-3, Obs2
	Proposed.v2	30	721	30.13	Thm1-3, Obs2
(7) All but L_9, L_{10}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	78	2092	11.14	Thm1-3, Obs2
	Proposed.v2	78	2092	11.14	Thm1-3, Obs2
(8) All latches L_1 to L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	1023	25252	7.62	Thm1-3, Obs2
	Proposed.v2	1023	25252	7.62	Thm1-3, Obs2

Table 14 Ten-stage T1 pipeline:
[DFT Config.5] (n,n), (n,s), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	12284	7.51	
	Previous.ext	10	220	100	
	Proposed.v1	10	220	100	-
	Proposed.v2	10	220	100	-
(2) L_3, L_{10}, L_{11}	Classical	1	12284	7.51	
	Previous.ext	10	350	55.60	
	Proposed.v1	14	300	86.23	Thm1-3
	Proposed.v2	14	300	86.23	Thm1-3
(3) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	30610	100	
	Proposed.v1	35	30610	100	-
	Proposed.v2	35	30610	100	-
(4) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	580	54.69	Thm1-3
	Proposed.v2	55	580	54.69	Thm1-3
(5) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	18352	25.51	
	Proposed.v1	45	820	64.52	Thm1-3
	Proposed.v2	45	820	64.52	Thm1-3
(6) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	19514	22.62	
	Proposed.v1	45	770	61.17	Thm1-3
	Proposed.v2	45	770	61.17	Thm1-3
(7) All but L_9, L_{10}	Classical	1	12284	7.51	
	Previous.ext	10	1452	10.65	
	Proposed.v1	78	4310	55.86	Thm1-3
	Proposed.v2	78	4310	55.86	Thm1-3
(8) All latches L_1 to L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	1023	147605	54.69	Thm1-3
	Proposed.v2	1023	147605	54.69	Thm1-3

Table 15 Ten-stage T1 pipeline:
[DFT Config.6] (n,n), (s,n), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	12284	7.51	
	Previous.ext	10	220	100	
	Proposed.v1	10	220	100	-
	Proposed.v2	10	220	100	-
(2) L_3, L_{10}, L_{11}	Classical	1	12284	7.51	
	Previous.ext	10	304	41.37	
	Proposed.v1	13	284	53.56	Thm1-3
	Proposed.v2	13	284	53.56	Thm1-3
(3) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	55	1456	7.62	Thm1-3
	Proposed.v2	55	1456	7.62	Thm1-3
(4) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	940	100	
	Proposed.v1	35	940	100	-
	Proposed.v2	35	940	100	-
(5) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	2538	22.62	
	Proposed.v1	45	736	25.61	Thm1-3
	Proposed.v2	45	736	25.61	Thm1-3
(6) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	2174	25.51	
	Proposed.v1	45	721	30.13	Thm1-3
	Proposed.v2	45	721	30.13	Thm1-3
(7) All but L_9, L_{10}	Classical	1	12284	7.51	
	Previous.ext	10	1452	10.65	
	Proposed.v1	78	2092	11.14	Thm1-3
	Proposed.v2	78	2092	11.14	Thm1-3
(8) All latches L_1 to L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	1023	25252	7.62	Thm1-3
	Proposed.v2	1023	25252	7.62	Thm1-3

Table 16 Ten-stage T1 pipeline: [DFT Config.7] (n,n), (n,s), (s,n), (s,s) in level-1 through level-9

Time borrowing sites (latch index)	Approach	No. of *SCUT*	No. of tests	Robust PDF coverage (%)	Reason(s) of test improvement from ITC03.ext
(1) None	Classical	1	12284	7.51	
	Previous.ext	10	220	100	
	Proposed.v1	10	220	100	-
	Proposed.v2	10	220	100	-
(2) L_3, L_{10}, L_{11}	Classical	1	12284	7.51	
	Previous.ext	10	320	100	
	Proposed.v1	13	320	100	-
	Proposed.v2	13	320	100	-
(3) L_1, L_3, L_5, L_7, L_9, L_{11}, L_{13}, L_{15}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	30610	100	
	Proposed.v1	35	30610	100	-
	Proposed.v2	35	30610	100	-
(4) L_2, L_4, L_6, L_8, L_{10}, L_{12}, L_{14}, L_{16}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	940	100	
	Proposed.v1	35	940	100	-
	Proposed.v2	35	940	100	-
(5) L_1, L_4, L_5, L_8, L_9, L_{12}, L_{13}, L_{16}, L_{17}	Classical	1	12284	7.51	
	Previous.ext	10	1270	100	
	Proposed.v1	35	1270	100	-
	Proposed.v2	35	1270	100	-
(6) L_2, L_3, L_6, L_7, L_{10}, L_{11}, L_{14}, L_{15}, L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	1200	100	
	Proposed.v1	35	1200	100	-
	Proposed.v2	35	1200	100	-
(7) All but L_9, L_{10}	Classical	1	12284	7.51	
	Previous.ext	10	1452	10.65	
	Proposed.v1	78	6360	100	Thm1-3
	Proposed.v2	78	6360	100	Thm1-3
(8) All latches L_1 to L_{18}	Classical	1	12284	7.51	
	Previous.ext	10	24514	7.51	
	Proposed.v1	1023	264600	100	Thm1-3
	Proposed.v2	1023	264600	100	Thm1-3

6. Conclusion

High-speed circuits use latch-based pipelines in some of their most delay-critical parts. The classical delay test methods, which are not supported by DFT for latch-based circuits, suffer from excessive test generation and test application times and, for many circuits, abysmally low fault coverage. Therefore, we introduced the first approach for structural delay testing of such circuits using a new type of DFT in [1] assuming a fully adaptive DFT approach.

The above fully adaptive DFT approach allows latches to operate in all combinations of modes, and is often not feasible due to its high DFT overheads, such as performance penalty, area overhead of latch designs with multi-functional DFT features, and routing of control signals as well as complex reconfigurable scan chains. Therefore, in this paper we propose a new test generation approach that optimizes the test quality under any available set of DFT configurations.

In order to overcome the limitations imposed by unavailable DFT configurations, three new techniques have been developed and implemented in the new test generator. We have also developed an approach that identifies the best available DFT configuration so that the sizes of target paths are minimized and a minimum number of *SCUTs* are tested. Extensive experiments demonstrate that our test approach, when applied under restricted DFT configurations, does not sacrifice much of the benefits of the fully-adaptive approach while significantly decreasing DFT overheads.

We are now carrying out detailed design of the DFT circuitry. Also, we are working on the problem of overall optimization of DFT design for latch-based high-speed pipelines with time borrowing, which involves the optimal design of configurations by considering the tradeoff between DFT overheads and robust coverage. We are also developing an approach to identify the *SCUTs* to be tested so as to minimize the average test application costs. Finally, we are extending our approach to general latch-based networks.

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