# Verifying RT constraints for GasP using PrimeTime

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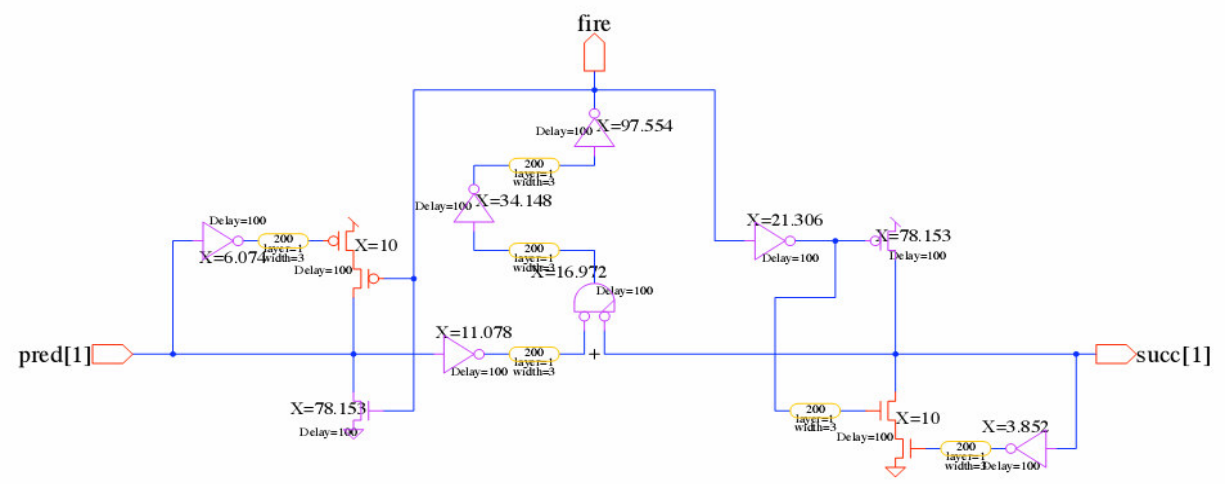
# Creation of GasP liberty file:

The first step in performing a Static Timing Analysis (STA) over any architecture is to create a timing model for the particular architecture. We chose to use the Synopsys Liberty Format (.lib) for representing the timing model because we are using Synopsys Primetime for STA. The following section describes the steps which were taken towards creation of the .lib.

## *GasP Architecture*

The following figure gives a pictorial description of the GasP Plain cell:




As depicted in the above figure, the GasP cells have two bidirectional pins namely the predecessor (P) and the successor (S), and one output pin which is the Fire (F) signal. It was my initial perception that since there exists an arc from P → F and also an arc from F → S, the pin F should be defined as an inout (i.e. bidirectional) in the .lib. In order to represent the behavior of the GasP cell, I created a fake .lib which had the GasP Plain cell with three bi-directional pins. This .lib along with a Verilog representation of a 5-stage linear pipeline was then given to Primetime for analysis. Using the report_delay_calculation command, I could identify the various arcs interpreted by Primetime.

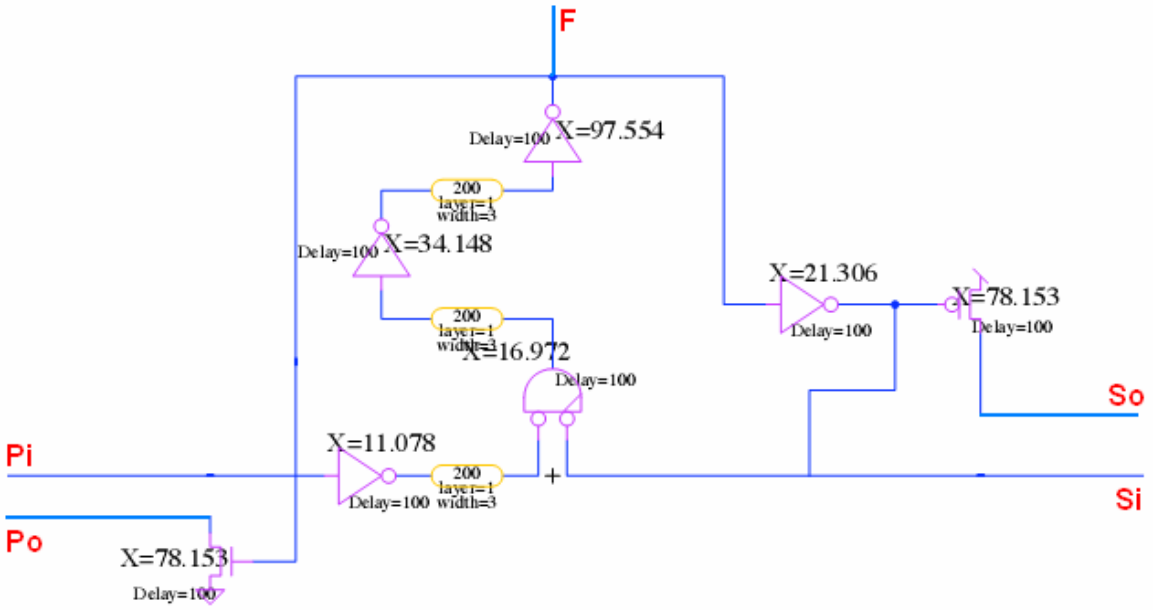
This command reported arcs from P → F and from F → S, but couldn't establish an entire path from P → S. As a result of this, I concluded the following:

1. The path was being cut at F

I also postulated that:

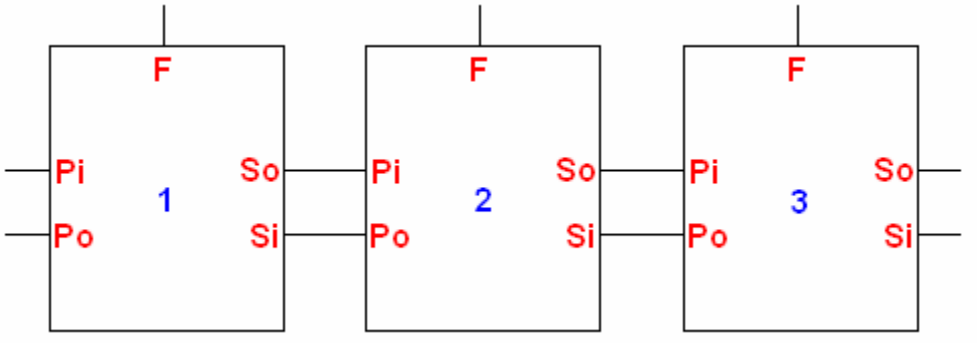
2. This problem could be due the presence of the bi-directional pins on the channels.

Assuming that the bidirectional pins on P and S were the problem, I created another .lib with pins on the channels being separated into 2 separate input and output pins. An abstract drawing of this split pin architecture is shown in the following figure:




The legend for the above figure is as follows:
Pi - input from Predecessor
Po - output to Predecessor
Si - input from Successor
So - output to Successor
F - Fire Signal

A typical 3 stage pipeline is shown in the following figure for a clearer understanding.




Equipped with the new .lib, I again ran Primetime on the same 5-stage pipeline. I had kept the F pin as an inout pin in this .lib as well. Again the result was the same as before. In this Primetime run as well, primetime recognized that there is an arc from Pi → F and also an arc from F → So, but it couldn't recognize the path between Pi → So.

Now, the conclusion was evident, that primetime was breaking the path at F. Upon inspection I found out that, whenever a pin in defined as an "inout", Primetime defines 2 ports, namely an input port and an output port for the same pin. It is also a characteristic

of Primetime to thereby cut timing paths within the same cell at all input ports. Hence the input(Pi)-to-output(So) was getting cut at input(F). To overcome this problem I had to define F as an output port. This solved the problem for both the .lib's created till now. It is important to note that Primetime has no problems accepting output-to-output arcs, which in this case will be from F → S.

I then used the corrected .lib which is same as the first one except for the change in the direction of pin F, for further analysis. Using check_timing command, I could identify the timing loops that are inadvertently present in the GasP design. These loops can be broken manually at the desired places using set_disable_timing. I was able to calculate the forward latency, by disabling the arcs on the backward path of the timing loops. Similarly the reverse latency of the design can be measured by disabling the arcs on the forward path.

Both the .lib's produced the exact same results and the bidirectional channel pins in the first design seemed to be working well.

## Verifying the Relative Timing (RT) constraints defined at USC

I then moved towards verifying the timing constraints, I had defined in the document Fleet_Analysis.V3.2. The far input loop constraint on the output channel (O-FIL) was arbitrarily chosen by me for verification. The two paths that need to be measured are as follows:

1. F+ → S+
2. F+ → P- → F- (or Fbar+)

The second path here clearly suggests that we want Primetime to verify the delay through a cycle without breaking it. This was not possible as Primetime will break the cycle and hence we will get incorrect numbers.

As suggested by Dr. Beerel, I created a fake pin named (Fclk) in the .lib to break the second timing path as follows:

F+ → P- → Fclk-

This new .lib still had the bidirectional pins at the channels. It has been my emphasis to try and make Primetime understand the bi-directional pins as much as possible. The Split pin architecture was the final resort.

In order to see, whether the different paths were created, I used report_delay_calculation and report_timing.

The STA approach developed by Mallika Prakash of USC was used to verify the above mentioned constraint as follows:

1. Create a clock pin on the POD

2. Verify the difference between the two paths using set_data_check

For trial purposes, I created a clock on the F pin of the 2nd stage of the linear pipeline. When I used set_data_check on the 2 paths namely F+ → S+ and F+ → P- → Fclk-, I didn't get any results.

On further analysis I did report_timing on the path F → Fclk, and it showed me that there were no constraint paths. On explicitly specifying the path as rise_from F to fall_to Fclk, primetime showed me that the path doesn't exist. My conclusion from these observations is as follows:

1. Due to the presence of the bidirectional pin P in the path of F+ to Fclk-, Primetime breaks the timing path at P. Note that P also serves as "input" and primetime breaks timing paths internal to the cell passing through the "input" pins.
2. I need to make another .lib ☺

This new .lib had the bidirectional channel pins split into 2 pins and also had a separate Fclk pin as a fake pin for verifying the RT constraints. This .lib is shown in the Appendix A. I have also attached the Verilog file and the associated .tcl file in Appendix B and Appendix C respectively.

This .lib allows us to verify all the timing constraints that were defined in the document Fleet_Analysis.V3.2. The timing reports for the four major constraints can be seen in Appendix D-G.

**Future Tasks:**

Establish a similar flow to verify that GasP control circuits meet the relative timing constraints for the data latches.

# Appendix A (The final .lib !!!)

```
library(GASP2) {
technology(cmos);
delay_model : table_lookup;
library_features(report_delay_calculation);

time_unit : "1ns";
capacitive_load_unit (1.0,ff);
voltage_unit : "1V";
current_unit : "1uA";
pulling_resistance_unit : "1kohm";
leakage_power_unit : "1nW";


slew_upper_threshold_pct_rise : 70;
slew_lower_threshold_pct_rise : 30;
slew_upper_threshold_pct_fall : 70;
slew_lower_threshold_pct_fall : 30;

input_threshold_pct_rise : 30;
input_threshold_pct_fall : 70;
output_threshold_pct_rise : 30;
output_threshold_pct_fall : 70;

nom_process : 1;
nom_voltage : 1.8;
nom_temperature : 25;

default_leakage_power_density : 0.0;
default_cell_leakage_power : 0.0;
default_fanout_load : 1.0;
default_output_pin_cap : 0.0;
default_inout_pin_cap : 0.0;
default_input_pin_cap : 0.0;

operating_conditions (typical) {
      process : 1;
      voltage : 1.8;
      temperature : 25;
}
default_operating_conditions : typical;

lu_table_template(delay_template_cap_P_plain_6x1) {
      variable_1 : total_output_net_capacitance;
      index_1 ("10,15,20,25,30,35");
}

lu_table_template(delay_template_P_rise_plain_6x1) {
      variable_1 : input_net_transition;
      index_1 ("0.1,0.2,0.3,0.4,0.5,0.6");
}

lu_table_template(delay_template_P_fall_plain_6x1) {
      variable_1 : input_net_transition;
      index_1 ("0.1,0.2,0.3,0.4,0.5,0.6");
```

```
}

lu_table_template(delay_template_S_rise_plain_6x1) {
      variable_1 : input_net_transition;
      index_1 ("0.1,0.2,0.3,0.4,0.5,0.6");
}

lu_table_template(delay_template_S_fall_plain_6x1) {
      variable_1 : input_net_transition;
      index_1 ("0.1,0.2,0.3,0.4,0.5,0.6");
}

lu_table_template(delay_template_cap_S_plain_6x1) {
      variable_1 : total_output_net_capacitance;
      index_1 ("10,15,20,25,30,35");
}

cell(GASP_PLAIN) {

      cell_leakage_power : 0.0;

      pin (Pi) {
            direction : input;
            capacitance : 10;
            }

      pin (Po) {
            direction : output;
            capacitance : 10;

            timing() {

                  related_pin : "F";
                  timing_type : combinational_fall;
                  timing_sense : negative_unate;
                  cell_fall(delay_template_cap_P_plain_6x1) {
                        values("1,2,3,4,5,6");
                        }
                  fall_transition(delay_template_cap_P_plain_6x1) {
                        values("0.1,0.2,0.3,0.4,0.5,0.6");
                        }
                  }
            }

      pin (F) {
            direction : output;
            capacitance : 10;

            timing() {

                  related_pin : "Pi";
                  timing_type : combinational_rise;
                  timing_sense : positive_unate;

                  cell_rise(delay_template_P_rise_plain_6x1) {
                        values("1,2,3,4,5,6");
                        }
```

```
            rise_transition(delay_template_P_rise_plain_6x1) {
                  values("0.1,0.2,0.3,0.4,0.5,0.6");
                  }
            }

      timing() {

            related_pin : "Si";
            timing_type : combinational_rise;
            timing_sense : negative_unate;
            cell_rise(delay_template_S_rise_plain_6x1) {
                  values("1,2,3,4,5,6");
                  }
            rise_transition(delay_template_S_rise_plain_6x1) {
                  values("0.1,0.2,0.3,0.4,0.5,0.6");
                  }
            }
      }

pin (Fclk) {
      direction : output;
      capacitance : 10;


      timing() {

            related_pin : "Po";
            timing_type : combinational_fall;
            timing_sense : positive_unate;

            cell_fall(delay_template_P_fall_plain_6x1) {
                  values("1,2,3,4,5,6");
                  }
            fall_transition(delay_template_P_fall_plain_6x1) {
                  values("0.1,0.2,0.3,0.4,0.5,0.6");
                  }

            }

      timing() {

            related_pin : "So";
            timing_type : combinational_fall;
            timing_sense : negative_unate;

            cell_fall(delay_template_S_fall_plain_6x1) {
                  values("1,2,3,4,5,6");
                  }
            fall_transition(delay_template_S_fall_plain_6x1) {
                  values("0.1,0.2,0.3,0.4,0.5,0.6");
                  }
            }
      }

pin (Si) {
      direction : input;
      capacitance : 10;
```

```
            }

      pin (So) {
            direction : output;
            capacitance : 10;

            timing() {

                  related_pin : "F";
                  timing_type : combinational_rise;
                  timing_sense : positive_unate;
                  cell_rise(delay_template_cap_S_plain_6x1) {
                        values("1,2,3,4,5,6");
                        }
                  rise_transition(delay_template_cap_S_plain_6x1) {
                        values("0.1,0.2,0.3,0.4,0.5,0.6");
                        }
                  }

            }
      }
}
```

# Appendix B (verilog file for the linear pipeline)

```
module GASP_PLAIN (Pi,Po,F,Fclk,Si,So);

input Pi;
output F;
output Fclk;
input Si;
output Po;
output So;

endmodule


module GASP_PIPE(Pin,Pout,Sin,Sout);

input Pin;
output Pout;
input Sin;
output Sout;


wire
S1in,S1out,S2in,S2out,S3in,S3out,S4in,S4out,F1,F2,F3,F4,F5,F1c,F2c,F3c,
F4c,F5c;

GASP_PLAIN I1
(.Pi(Pin),.Po(Pout),.F(F1),.Fclk(F1c),.Si(S1in),.So(S1out));
GASP_PLAIN I2
(.Pi(S1out),.Po(S1in),.F(F2),.Fclk(F2c),.Si(S2in),.So(S2out));
GASP_PLAIN I3
(.Pi(S2out),.Po(S2in),.F(F3),.Fclk(F3c),.Si(S3in),.So(S3out));
GASP_PLAIN I4
(.Pi(S3out),.Po(S3in),.F(F4),.Fclk(F4c),.Si(S4in),.So(S4out));
GASP_PLAIN I5
(.Pi(S4out),.Po(S4in),.F(F5),.Fclk(F5c),.Si(Sin),.So(Sout));

endmodule
```

# Appendix C (final .tcl script used for verification)

```
set netlist gasp4.v
set top GASP_PIPE
read_lib gasp4.lib
read_verilog $netlist
set link_path "GASP2 $netlist"
echo $link_path
link_design -keep_sub_designs $top
check_timing -include loops -verbose


#uncomment to verify one of the following four constraints

#O-FIL
#set_disable_timing -from Si -to F [ get_cells -hierarchical * ]
#create_clock -period 10.0 I2/F
#set_data_check -clock I2/F -rise_to I3/Pi -fall_from I2/Fclk -setup
1.5

#I-FOL
#set_disable_timing -from Pi -to F [ get_cells -hierarchical * ]
#create_clock -period 10.0 I2/F
#set_data_check -clock I2/F -fall_to I1/Si -fall_from I2/Fclk -setup
1.5

#fwd short circuit (O-SC)
#set_disable_timing -from Si -to F [ get_cells -hierarchical * ]
#set_disable_timing -from F -to Po [ get_cells -hierarchical * ]
#create_clock -period 10.0 I2/F
#set_data_check -clock I2/F -rise_to I3/F -fall_from I2/Fclk -setup 0.5

#rev short circuit (I-SC)
#set_disable_timing -from Pi -to F [ get_cells -hierarchical * ]
#set_disable_timing -from F -to So [ get_cells -hierarchical * ]
#create_clock -period 10.0 I2/F
#set_data_check -clock I2/F -rise_to I1/F -fall_from I2/Fclk -setup 0.5

report_timing
```

# Appendix D (timing report for O-FIL)

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : GASP_PIPE
Version: A-2007.12-SP3
Date   : Thu Jun  5 16:52:41 2008
****************************************


  Startpoint: I2/F (clock source 'I2/F')
  Endpoint: I3 (falling edge-triggered data to data check clocked by
I2/F)
  Path Group: I2/F
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/So (GASP_PLAIN)                       3.00       3.00 r
  I3/Pi (GASP_PLAIN)                       0.00       3.00 r
  data arrival time                                   3.00

  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/Po (GASP_PLAIN)                       3.00       3.00 f
  I2/Fclk (GASP_PLAIN)                     3.00       6.00 f
  data check setup time                   -1.50       4.50
  data required time                                  4.50
  -----------------------------------------------------------
  data required time                                  4.50
  data arrival time                                  -3.00
  -----------------------------------------------------------
  slack (MET)                                         1.50


1
```

# Appendix E (timing report for I-FOL)

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : GASP_PIPE
Version: A-2007.12-SP3
Date   : Thu Jun  5 16:54:34 2008
****************************************


  Startpoint: I2/F (clock source 'I2/F')
  Endpoint: I1 (falling edge-triggered data to data check clocked by
I2/F)
  Path Group: I2/F
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/Po (GASP_PLAIN)                       3.00       3.00 f
  I1/Si (GASP_PLAIN)                       0.00       3.00 f
  data arrival time                                   3.00

  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/Po (GASP_PLAIN)                       3.00       3.00 f
  I2/Fclk (GASP_PLAIN)                     3.00       6.00 f
  data check setup time                   -1.50       4.50
  data required time                                  4.50
  -----------------------------------------------------------
  data required time                                  4.50
  data arrival time                                  -3.00
  -----------------------------------------------------------
  slack (MET)                                         1.50


1
```

# Appendix F (timing report for O-SC)

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : GASP_PIPE
Version: A-2007.12-SP3
Date   : Thu Jun  5 16:56:07 2008
****************************************


  Startpoint: I2/F (clock source 'I2/F')
  Endpoint: I3 (falling edge-triggered data to data check clocked by
I2/F)
  Path Group: I2/F
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/So (GASP_PLAIN)                       3.00       3.00 r
  I3/F (GASP_PLAIN)                        3.00       6.00 r
  data arrival time                                   6.00

  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/So (GASP_PLAIN)                       3.00       3.00 r
  I2/Fclk (GASP_PLAIN)                     3.00       6.00 f
  data check setup time                   -0.50       5.50
  data required time                                  5.50
  -----------------------------------------------------------
  data required time                                  5.50
  data arrival time                                  -6.00
  -----------------------------------------------------------
  slack (VIOLATED)                                   -0.50


1
```

# Appendix G (timing report for I-SC)

```
****************************************
Report : timing
      -path_type full
      -delay_type max
      -max_paths 1
Design : GASP_PIPE
Version: A-2007.12-SP3
Date   : Thu Jun  5 16:57:19 2008
****************************************


  Startpoint: I2/F (clock source 'I2/F')
  Endpoint: I1 (falling edge-triggered data to data check clocked by
I2/F)
  Path Group: I2/F
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/Po (GASP_PLAIN)                       3.00       3.00 f
  I1/F (GASP_PLAIN)                        3.00       6.00 r
  data arrival time                                   6.00

  clock I2/F (rise edge)                   0.00       0.00
  clock source latency                     0.00       0.00
  I2/F (GASP_PLAIN)                        0.00       0.00 r
  I2/Po (GASP_PLAIN)                       3.00       3.00 f
  I2/Fclk (GASP_PLAIN)                     3.00       6.00 f
  data check setup time                   -0.50       5.50
  data required time                                  5.50
  -----------------------------------------------------------
  data required time                                  5.50
  data arrival time                                  -6.00
  -----------------------------------------------------------
  slack (VIOLATED)                                   -0.50


1
```