

A CMOS Implementation of Neural Dendritic Computations with Cost Analysis

Alice C. Parker, Jonathan Joshi, Waleed Dweik,
Jameel Koita, Nav Aman Deep Singh
EE Department, University of Southern California
Los Angeles, CA, US
parker@eve.usc.edu

Olanrewaju Ayo
Novelics
Aliso Viejo, CA, US

Abstract— Modeling the dendritic arbor of a cortical neuron is important because each dendritic arbor contains thousands of synapses along with dendritic computations on the signals generated by the synapses in the arbor. Nanometer-scale CMOS circuits, important for the scale of future synthetic neural systems, also raise the inherent issue of power consumption. This paper explores the cost of implementing basic dendritic arbors in terms of area and power consumption. The dendritic computational components used are capable of linear and non-linear summations and are simulated in SPICE to show biomimetic capability. A comparison of possible components is presented to illustrate the possibilities of implementation.

I. INTRODUCTION

One of the most difficult of the challenges in modeling the cerebral cortex is the massive scale. Cortical neurons possess an average of 10,000 and up to 100,000 synaptic connections (neural inputs)[1][2]. Each synaptic connection is found on a dendritic arbor, a tree structure that performs computations on the signals generated by the synapses. With approximately 100 billion neurons in the human cortex, and approximately 60 trillion synaptic connections, connectivity between neurons and within each neuron in a synthetic brain cortex will be a major challenge. In recent years, several artificial brain projects have been launched that rely on computer simulations of neural behavior on multiprocessors, such as the IBM artificial brain project in cooperation with EFPL [3]. These simulations are large and slow, however, with each processor simulating a single neuron, and with simulations running well behind real time, even for small brain portions. Many researchers believe that emulation with custom electronic circuits can have several advantages over simulation, generally being faster and smaller, sometimes running at nearly real time for small problems.

The dendritic arbor is one of the most complex parts of the neuronal structure in terms of biomimetic modeling. A single node can fan out to several presynaptic connections, or several synapses can form around a single node. Multiple synapses can converge (fan in) to a single node, either from a single oversized presynaptic terminal or from multiple presynaptic terminals. Dendritic trees can influence the growth of new

connections, either by sharing ion flow, or by forming synaptic connections. Dendritic trees form the bulk of a cortical structure [2].

With CMOS scaling over the next decade, it might be possible to achieve modeling of dendritic trees that meets the numerical challenges of an artificial cortex. The success of an artificial cortex will be determined not only by meeting the goal of scale but also by managing its power consumption.

An important question that leads to the success of a Biomimetic CMOS implementation is the level to which the major features of neural behavior are considered. The consequences of pursuing intricate biomimetic behavior are high transistor count and subsequent power consumption, increasingly due to leakage.

This paper considers the factors that could lead to obstacles in the implementation of a CMOS dendritic tree. This paper discusses cost factors concerning dendritic components: namely analog adder structures, that appear to be the most common computations in dendritic structures, apart from inhibitory activities. We have implemented several dendritic tree portions, using adder circuits capable of adding Electronic Post Synaptic Potentials (EPSPs) and have simulated them in SPICE to show biomimetic capability and utility in neuronal circuits. We provide a comparison of these implementations using the costs of power and transistor gate area, and project the increase in power consumption that results from the numerical increase of dendritic complexity.

II. BACKGROUND

Hynna and Boahen report on a circuit that generates a calcium spike with attention paid to exact replication of waveforms, and describe incorporation of the calcium spike circuit in an entire neuron circuit [4]. Elias modeled dendritic computations as early as 1992 [5]. Hasler and Farquhar also model dendritic transmission [6],[7], as do others (e.g. Arthur [8] and Rasche [9]). These papers discussed the biomimetic implementations and focused more on the exact replication of waveforms.

The first extensive exploration of cost towards building artificial neurons was given by Parker [10] with respect to the interconnectivity and the transistor count. Here, the question that is being posed is analogous to the current focus in conventional CMOS circuits: that of power. Wen and Boahen [11] show a cochlear amplifier where power was examined. Taba and Boahen [12] also talk about a low power implementation in comparison to a software simulation. Lazzaro has implemented low-power neurons [13]. However, dendritic trees have not been the focus of low-power neural design activity. With the number and size of dendritic trees in the brain, exploration of their power consumption is critical.

III. DENDRITIC COMPUTATION MODULES

The two dendritic computational modules implemented are analog CMOS adders capable of biomimetic dendritic computations. The adder circuits were selected on the basis of their biomimetic characteristics, including the ability to create sublinear and superlinear summations like those found in biological neurons. Adders using operational amplifiers were not considered since their analogy to biological neural structures was not as clear.

The first voltage adder (Fig. 1) uses voltage-to-current conversion, current summing, current mirroring and current-to-voltage conversion [14]. The circuit is low in power, with few transistors, and low harmonic distortion.

The second adder is a typical CMOS analog adder used for signal processing applications [15]. This adder exploits the square law relationship between gate voltage and drain current with good linearity and accuracy and wide input and output range. Multiple current mirrors are used to correct for non-linearity, making this circuit about 27% larger in total gate area than the silicon area of the basic adder.

Fig. 2 illustrates the basic CMOS synapse we have developed that creates the inputs to the dendritic arbor when pre-synaptic neurons connected to the synapses fire action potentials [16].

IV. DENDRITIC NETWORK AND EXPERIMENTS

A block diagram of the dendritic arbor portion is shown in Fig. 3. There are four synapses in the arbor, each on a separate dendritic branch. We do not include the active area of the synapse circuit as it is equally present in dendritic arbors containing both the computational modules. We ran a number of simulation experiments with each adder, in order to illustrate the use of the adders for linear, sublinear and superlinear addition of the Excitatory PostSynaptic Potentials (EPSPs), and varying the number of action potentials in each time period in order to observe any differences in power consumption. The basic adder is also capable of sublinear and superlinear summations, as we have shown earlier using carbon nanotube transistor SPICE models [17].

Figure 4 illustrates the response of the synapse tree with our basic adder 1 to four action potentials arriving at synapses, and the resultant four postsynaptic potentials being summed linearly. Figure 5 illustrates the response of the synapse tree with adder 2 to the same inputs. Figure 6 illustrates the

sublinear and superlinear additions possible in the adder tree using adder 2 with modifications.

V. MEASURING AND PREDICTING AREA AND POWER

Care has been taken in the design of the synapse circuit and the selection of adder circuits to achieve a high level of biomimeticity. This degree of biomimeticity comes with a cost, that may be great enough to preclude large-scale synthetic neural structures in the next several decades.

The cost analysis for our dendritic tree is based on transistor gate area and average power dissipation as measured by SPICE. We assume a standard figure of 10,000 summation nodes per dendritic arbor [2] and scale the power dissipated for each adder component.

This is an absolute worst-case cost as the switching activity (based on neuron firing rate) is significantly less than 100% in many regions of the brain; further insight on firing rates is being investigated. Since the circuits are not digital, the variation between power consumed in the presence of action potentials and without input action potentials is insignificant in a sample of the cases.

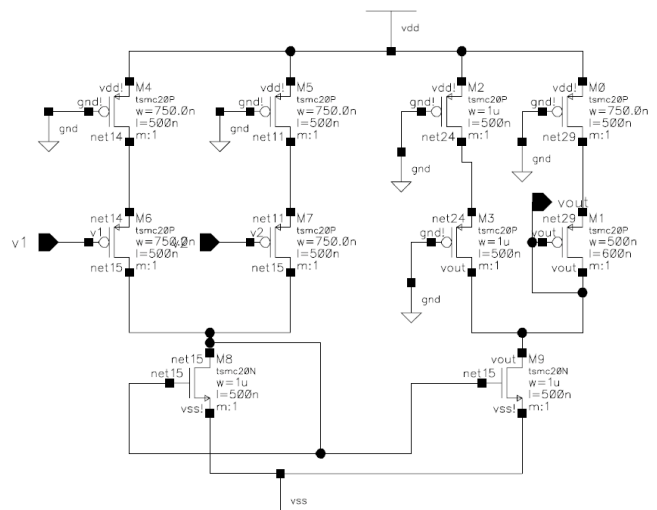


Figure 1 The basic voltage adder [14]

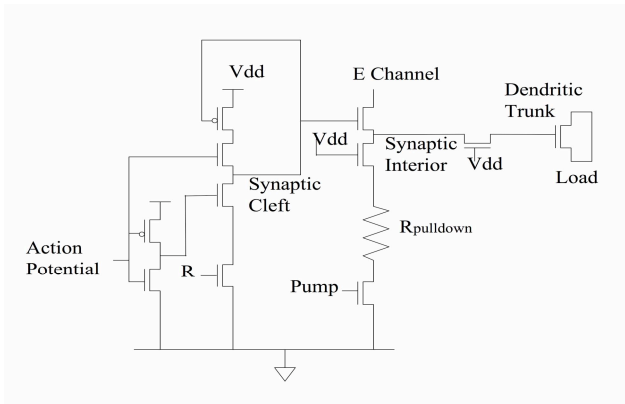


Figure 2: The CMOS synapse [16]

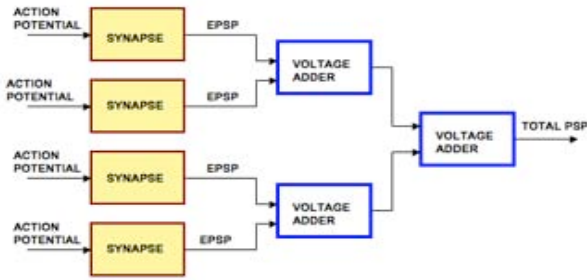


Figure 3: The dendritic arbor portion

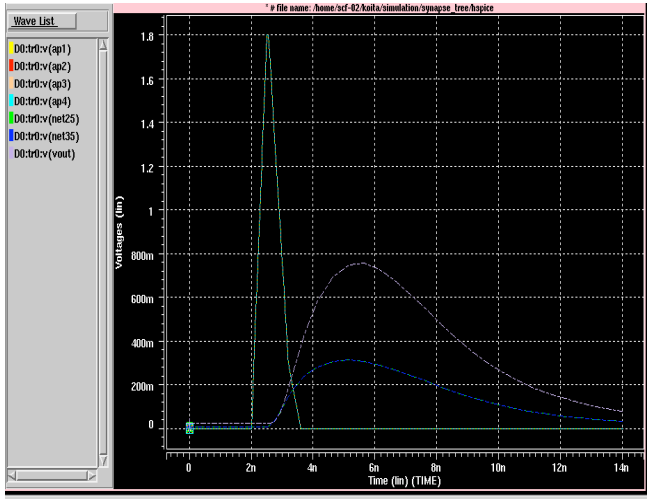


Figure 4: The synapse tree output with adder 1, with four action potentials

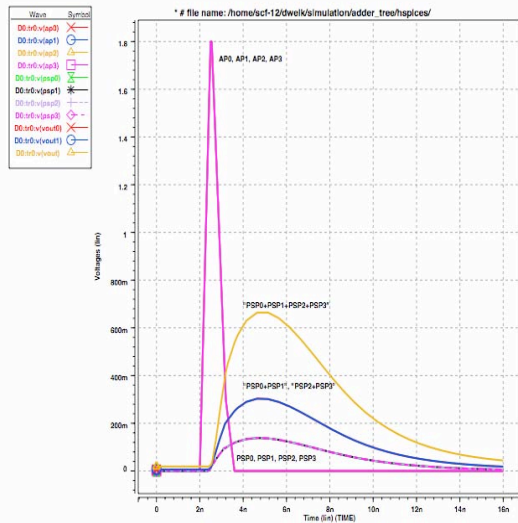


Figure 5: The synapse tree output with adder 2, with four action potentials

This cost helps us to understand the trade off between implementing biomimetic behavior versus transistor count and power.

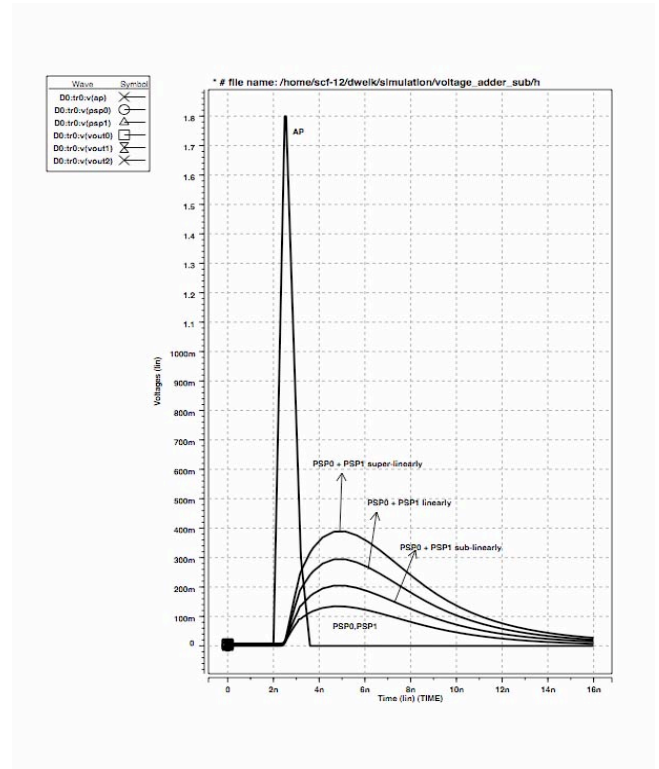


Figure 6: The synapse tree output with adder 2, showing sublinear and superlinear addition

Table 1 contains the total gate area for each adder implementation, and the average power consumed over a 2ns window when the action potential at the input to each synapse is spiking. The table also shows the gate area and predicted average power in 2021, based on International Technology Roadmap [18] parameters. Scaling to biological voltages could also be possible, and so a third set of entries in the table shows predicted average power in 2021 assuming voltages have been scaled to neural biological levels. Projecting to 2021, the International Technology Roadmap predicts a V_{dd} of 0.45 v., and a proportionally scaled drain current would decrease by a factor of 4 from our current 180nm technology in an NMOS device.

This scaling itself would provide a reduction in power of 1/16 per device over current estimates. While scaling and the introduction of high-K dielectrics complicate leakage power predictions, we are simply assuming for this preliminary analysis that power per device scales by $1/s^2$ for comparison purposes.

In addition to the reduction in power due to device scaling, an even more important adjustment to circuit voltages is likely to occur, the scaling of voltages to biomimetic levels. If V_{dd} in 2021 is 0.45 v., then our circuits as presently implemented would assume action potentials of around 0.45 v. at their peak, and would produce EPSPs with peak voltages of about 10% of V_{dd} , or 0.045 v. Biological neurons have actions potentials with about 100 mv. of magnitude variation, and excitatory post synaptic potentials on the order of 10 mv. In order to scale our neurons in 2021

to biomimetic levels, the action potential and excitatory postsynaptic potential voltages would be further scaled by a factor of about 1/(4.5), or to about 22.2% of the unscalded 2021 voltages. As a result of this scaling, all transistor operations would become subthreshold. The log of current would scale proportional to the voltage in this weak inversion regime [19]. Hence the current would scale in the following manner:

$$I_{d\ 2021} = (I_{d\ 2021\ \text{biomimetic}})^{4.5} \quad (1)$$

$$\text{Where } I_{d\ 2021} = P_{2021}/V_{2021} \quad (2)$$

VI. DISCUSSION

Our future power predictions were performed by simple scaling of power by $1/s^2$ where our value of s was 4 from our current 180nm technology to the ITRS technology predictions in 2021. Once we obtained this power prediction, however, we speculated whether the scaling of the brain to biological voltages would make a significant difference in power predicted. We computed the total current by dividing the power by the supply voltage, 0.45 volts. We scaled the maximum voltage to 100mv, commensurate with the change in potential when biological neurons fire. Recognizing that the log of the drain current would decrease linearly with V_{GS} [19], we scaled the current accordingly. We then computed the biological (biomimetic) power consumption by multiplying scaled voltage by scaled current.

Our power predictions per neuron are a concern, considering the estimate of 100 billion neurons in the cortex. We assume for these simple predictions that the high-K dielectrics will prevent further increases in gate leakage power through 2021. The power results illustrate that the scale of a synthetic cortex, even in 2021, will present immense power requirements, making such a hardware implementation with full dendritic computational capability impractical. The importance of dendritic computations in neural computations has been cited by many neuroscientists.

We have shown that the power cost of such dendritic computations is significant when performed in a manner that allows the control of the computations to range from sublinear to superlinear additions. Constructing a synthetic cortex using

TABLE 1 COSTS OF THE ADDERS OVER TIME AND WITH SCALING TO BIOLOGICAL VOLTAGES.

Cost	Synapse	Adder 1	Adder 2	Neuron using Adder 1	Neuron using Adder 2
Area (μm^2)	12.23	4.175	5.29	13,915	17,653
Power 190nm (watts)	1.958×10^{-5}	116.8×10^{-5}	14.40×10^{-3}	3.986	48
Power 2021 (watts)	0.121×10^{-5}	7.45×10^{-5}	90.1×10^{-3}	.249	3.005
Power 2021 (Bio) (watts)	0.0625×10^{-5}	2.63×10^{-5}	4.575×10^{-5}	0.08766	.1525

CMOS technology seems to be infeasible when power is taken into consideration.

We have not factored in computations that occur when some postsynaptic potentials are inhibitory. We believe that if similar cost were to be incurred for dendritic computations containing hyperpolarizing inhibitory postsynaptic potentials, our predictions for neural costs would still hold.

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