

Unified System Construction (USC) Tools

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This brief report summarizes software tools developed as part of the Unified Systems Construction Project.

I. ADAM High-Level Synthesis Tools for Single - Chip Designs

VHDL2DDS - Translator from VHDL to the ADAM format for behavioral/structural VHDL.

MAHA - Schedules behavioral VHDL to produce non-pipelined datapaths which either minimize cost subject to timing constraints or minimize delays subject to cost constraints.

Sehwa - schedules behavioral VHDL to produce pipelined datapaths which either minimize cost subject to timing constraints or minimize delays subject to cost constraints. (The C version of Sehwa is available from UC Irvine and is recommended.)

LADS - schedules and partially allocates behavioral VHDL, while simultaneously floor-planning to minimize interconnect delays. An earlier version was called 3D-scheduling. Separate routines, in conjunction with LADS, model thermal effects.

MABAL - allocates multiplexers, bus drivers, buses, registers and functional units to complete the register-transfer datapaths produced by MAHA, Sehwa and other scheduling programs.

CSG - Control Signal Generator which constructs a state machine (state table) for the datapaths produced in ADAM, given a control flow graph.

SLIMOS - selects module styles for functions specified in VHDL. Most appropriate for pipelined designs. Executes before high-level synthesis, using the behavioral specification.

CONSPEC - Control Specifiers constructs a state machine (state table) for designs with complex timing constraints (e.g. I/O interfaces), given a datapath and control flow graph.

II. ADAM High-Level Synthesis tools for Multi-Chip Designs

A. Systems with Synchronous Interchip Communication

CHOP - Evaluates and performs “what-if” prediction for multiple behavioral partitions with real-time constraints; automatically performs two-way partitioning; selects design style, module style, and amount of parallelism for each partition.

SMASH - Synthesizes memory-intensive datapaths along with on-and off-chip memory structures.

MCS - Schedules datapaths across multiple chips with synchronous I/O and constructs interconnect architecture.

B. Systems with Asynchronous Interchip Communication

PROPART - Automatically partitions behavioral specification consisting of multiple processes onto one or more chips; selects process features.

Synthesizes integrated concurrent datapaths on multiple chips.

III. ADAM High -Level Prediction Tools

PLEST - predicts standard cell wiring space from the parameters of the register-transfer design. (accurate to 10% for 1.2u CMOS).

PASTA - predicts PLA size for controllers from state machine specification. (accurate to 10% for 1.2u CMOS)

BEST - predicts die area and performance from a behavioral specification. Takes into account datapaths (functional, register, multiplexer and bus driver) area and delay, controller area and delay, and wiring space area and delay. (accurate to 10% for 1.2u CMOS on selected examples).

IV. ADAM Framework Tools

EVE - object-oriented database shell constructed on a relational database, SUN unify.

SIN - X windows System Interface for the ADAM tools.

DPE - Design Process Engine controls the design process in the ADAM system, automatically selecting tools in order to achieve multiple goals (e.g. cost, performance,

design time).(currently not operational due to obsolence of the programming language Franz LISP - being rewritten).

V. System - Level Tools

PHRAN-SPAN - a natural language interface which converted system specification written in English into the USC internal format, the DDS (Design Data Structure). (currently not operational due to obsolence of the programming language Franz LISP - being rewritten).

SOS - A family of tools for synthesizing application - specific multiprocessor architectures and task schedules. Specific tools synthesize non-pipelined point - to point, bus, and ring architectures and pipelined point-to-point architectures.

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