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**System-Level Estimation
of Energy and Power**

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Abstract

We present a novel technique to predict energy and power consumption in an electronic system given its behavioral specification and library components. All feasible designs are investigated and the designer may tradeoff between low cost, high speed, low energy and low power. Our technique correlates the switching activity with the switching capacitance. Although, the predictions are performed prior to synthesis, the results are within 15% accuracy of power estimates performed on synthesized layouts.

1 Introduction

With the recent proliferation of applications in mobile computations and communications, research in low-power system design has become important. Several power prediction as well as minimization techniques at various stages of circuit specification, from low, transistor-level to high, RT-level are available [1–8]. However, as electronic systems become more complex, predictions at an even higher level of abstraction, namely the system-level are very useful. System-level predictions are made before making any design decisions including task-graph partitioning, selection of design styles for implementing each partition, relative scheduling of tasks, and synthesis of the inter-chip communication interface. These

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decisions influence the resource requirement of the resulting design, thereby influencing the power consumption in addition to cost and performance.

Accurate estimation of power at the system-level is crucial also during synthesis of a system in order to search the design space efficiently and to avoid design decisions that are likely to lead to high-power or high-energy designs. Unfortunately however, accurate power estimation requires detailed information regarding the physical design aspects of the system, and these estimates are not available at the system level. In this report, we present a statistical technique to estimate power for each task in a system which replaces detailed knowledge of the physical layout of the design with a statistical model relating (a) the lengths of two-point nets in the resulting design and (b) the switching activities on the wires. By correlating (a) and (b), we show how power and energy consumption in a system can be roughly estimated directly from its behavioral description without taking any synthesis steps.

The report is organized as follows. Previous work in the area of power estimation for digital circuits is surveyed in Section 2. An overview of our approach is given in Section 3. Section 4 describes the theoretical basis and mathematical model of our estimation algorithm. Experimental results are presented in Section 5, followed by conclusions in Section 6.

2 Previous Work

The well-known predictors PowerMill [1] and SPICE require a transistor-level description of the circuit. Najm [2], Ghosh *et al.* [3] and Marculescu *et al.* [4] have presented estimation techniques at the gate level. Since CMOS circuits consume or dissipate power only during switching, these techniques primarily emphasize accurate modeling of the switching activity in the circuit. At the architecture or RT level also, the focus remains on accurate yet faster modeling of the switching activity. Speed of estimation becomes important as the circuit size grows larger, from a few hundred gates to several thousand gates. Many of these approaches are entropy based [5] or information theoretic [6]. Power consumption by the interconnect is significant in a chip and was considered by Landman and Rabaey [7] and Liu and Svensson [8]. Although the RT level is a high level of abstraction, the designer must complete some of

the important steps of synthesis namely, scheduling, operator allocation and binding, before an architecture becomes available. Thus, the predictions performed apply to a single RT-level design in the design space. In order to explore the entire design space using RT-level power estimators, the above mentioned synthesis steps must be repeated several times. The process of searching for a low-energy or low-power design thus becomes time consuming. Behavioral-level predictions allow the designer to significantly decrease the number of actual RTL designs he or she must examine.

3 Behavioral system-level predictions

We first estimate the characteristics of possible system designs. Consider the Task Flow Graph (TFG) representation of a system as shown in Figure 1. Each task is associated with a Control Data Flow Graph (CDFG)¹, and we assume that it is implemented on one or more chips. The implementation style for each task could be different, such as semi-custom ASIC, FPGA, or off-the-shelf component. Considering all the options available for implementation, the feasible design space is extremely vast at the specification level. A system composed of these chips or dies is assembled on a PC board or an MCM or a combination of the two. For off-the-shelf components such as dynamic RAMS, cost, delay and power consumption are known. Our predictor estimates these attributes for undesigned tasks as described below.

Estimation of many of the system characteristics is provided by BEST [10]. Given the behavioral description of a task (CDFG) and a library of modules to be used for synthesis, many designs are feasible depending upon the area and timing constraints. Under tight area constraints, the resulting design tends to be *serial* as it has a small number of functional units. On the other hand, under strict timing constraints, the resulting designs are *parallel* or have a large number of functional operators. A formal method to predict each of these designs was introduced in BEST [10]. In a nutshell, BEST investigates all feasible execution delays (expressed in number of steps of clock cycle) for a given task, based on critical path analysis. Then, corresponding to each delay, the required number of functional operators of each

¹ This can be derived from a VHDL description, or composed from two directed graphs in the DDS internal representation: the data-flow graph and the the control and timing graph [9].

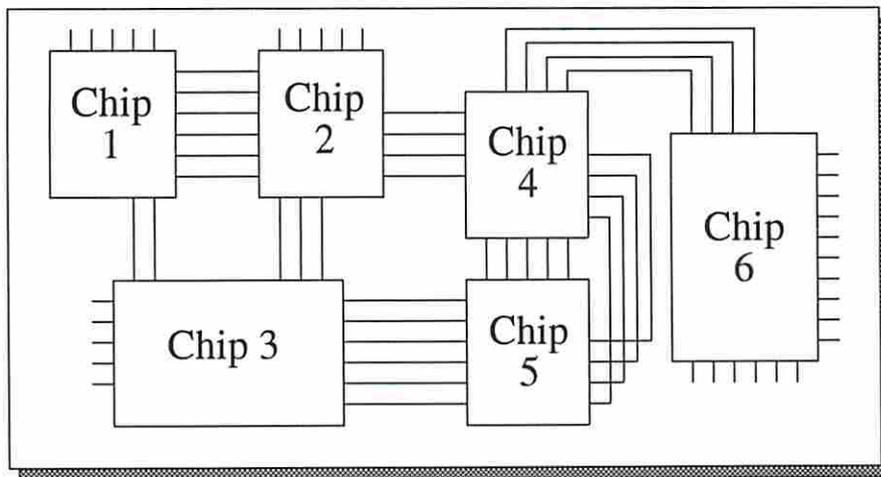
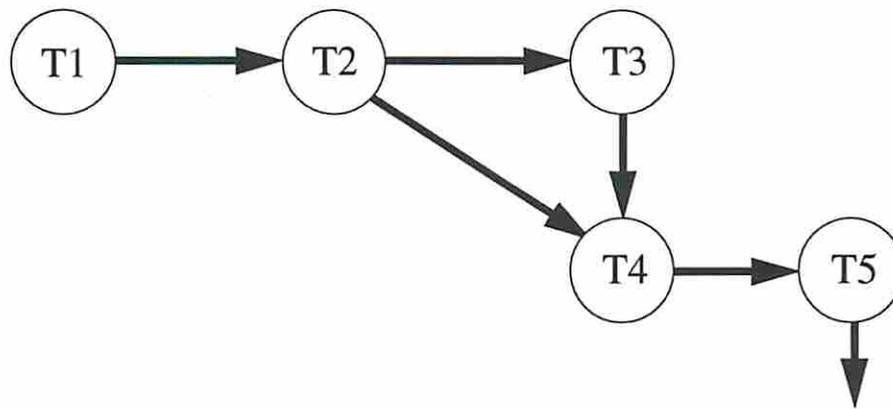


Figure 1: System Task-Flow Graph and implementation

type, multiplexers, registers and 2-point nets are predicted. We use the predicted designs generated by BEST as a starting point in our analysis. Figure 2 shows the overall prediction method.

After BEST, functional operator energy estimation is performed. Functional operators used in chips typically consist of a few hundred gates. In semi-custom ASIC design, these are pre-synthesized as macro cells. Thus, we have an *a priori* knowledge of the internal structure of these cells. Specifically, we know the number of standard cells or gate array cells used, the number of internal nets and physical dimensions. For each macro cell, we predict energy consumption by predicting the internal wire-length distribution using Kurdahi's model [11] and the associated switching capacitance. Here *internal* implies the nets connecting the constituent cells or gates of the macro cell. In this novel technique, we model a functional unit as a collection of nets with varying switching activity and capacitances. Correlation of the latter two is illustrated in Section 4.1.2. Accuracy of the results is improved by considering how frequently operators of each type are used.

Finally, energy consumed by the interconnect is estimated. As mentioned earlier, the number of external 2-point nets for a design is estimated by BEST. Here, *external* implies inter-functional-unit nets. In addition, from BEST we also know the number of operators of each type and their physical dimensions. Using this information and Kurdahi's model for wire-length distribution, we predict energy consumed by the external nets. The addition of all these components yields the total energy consumed by the chip for the predicted design being considered. We also know the execution delay for this design thus, we compute the average power consumption.

Estimation of the average wire length inside a functional component as well as in the target chip is critical in our method because, that is the only parameter that characterizes the geometric interconnect distribution. Statistical information on interconnects has been used in the past to predict area and delay. Zimmerman [12] proposed a slicing tree algorithm to predict routing area in standard cell designs by predicting wire lengths. This approach is computationally intensive. In addition, a typical chip consists of macro cells or clusters of rows of standard cells as opposed to a uniform placement throughout the chip area. Ramachandran and Kurdahi extended Zimmerman's approach to predict delays on the nets

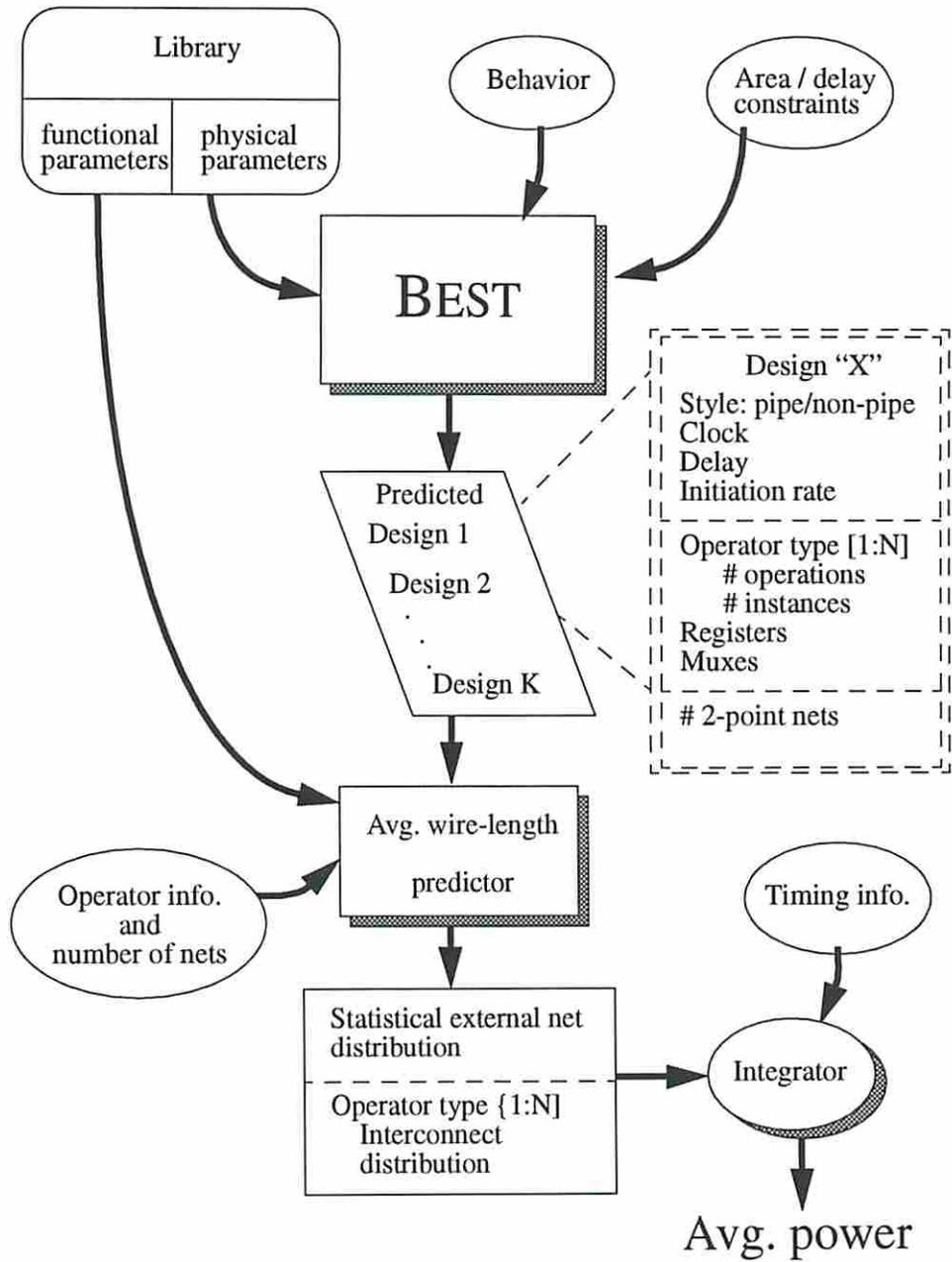


Figure 2: System-level power prediction

connecting macro cells [13]. In FASOLT by Knapp, wiring information was generated through a LAYOUT ESTIMATOR for macro cells [14]. While these techniques estimate the average wire length accurately, they start with an RT-level description of the circuit. Given a predicted design, we only know the expected number of operators of each type. Their connectivity is still unknown. Hence, we use interconnect length analysis based on Rent's rule.

4 Statistical power estimation

On a chip, power is consumed by

1. functional units such as multipliers, shifters, and adders,
2. storage and flow control units such as registers and multiplexers, and
3. nets connecting various functional units.

In our analysis, the only distinction we make is between the nets and all other modules. Therefore, in the mathematical model, functional units also include registers and multiplexers. A mathematical formulation for power consumption corresponding to a predicted design is given below.

4.1 Estimating power consumption of a functional unit

4.1.1 Background

The problem of estimating power consumption of a functional unit comprises two main sub-problems. First, one must estimate all the switching capacitances associated with the circuit accurately and next, the average switching activity for each one of those capacitances must be estimated. As mentioned earlier, Najm, Ghosh, and Marculescu have proposed methods to precisely estimate the latter [2–4]. Their methods are either probabilistic or statistical and they assume *a priori* knowledge of the switching activity on the primary inputs of the circuit. The first component, the set of all switching capacitances, is a characteristic of the circuit layout. It is typically obtained from the component library used in the

layout and the circuit topology. In the case of small functional units, comprised of a few standard cells (gates in a gate array design), the interconnects between the cells are short and the switching capacitance is dominated by the transistor gate and source/drain capacitances. However, in large functional units, routing capacitance between cells is comparable to gate input/output capacitances and hence, cannot be ignored.

4.1.2 Switching nets model

Switching capacitances

We model any functional unit as a collection of wires and standard cells (or gates in a gate array design). The numbers of wires and cells in a given unit are fixed and known. Dimensions of the unit are also known. Assuming standard cell placement, the average length of a wire in the unit is given by Feuer's formula as implemented by Kurdahi [11]. The average load on a wire depends on the average input/output capacitance of the standard cells. Thus, the total switching capacitance associated with each wire consists of

1. average load capacitance,
2. average internal capacitance of the standard cells, and
3. capacitance of the wire.

Items 1 and 2 are obtained from the standard cell library while item 3 depends on the length of the wire. For standard cell placement, the wire length distribution was shown to be geometric by Kurdahi [11], and we also assume the distribution is geometric.

Switching activity

Recall that our estimator starts with a behavioral description of the task and predicts power for all feasible designs. The procedure to estimate power for one functional unit must be fast because several designs are to be explored and each may consist of many functional units. In our approach, we make the following assumptions regarding the switching activity:

1. A good placement and routing algorithm is expected to place cells that share ports together. Thus, most short wires are likely to have high switching activity.
2. Many of the long wires carrying information such as clocks or multiplexer control are also likely to have high switching activity.
3. Medium length wires are likely to have relatively low switching activity.

A typical wire-length switching activity relation is shown in Figure 3.

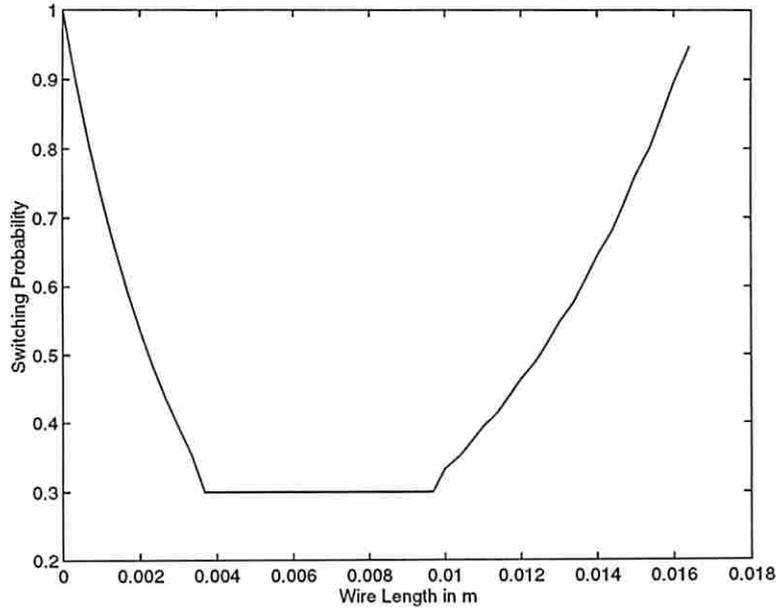


Figure 3: Wire-length switching activity relation

Mathematical model

We have created an empirical model for switching activity, heavily influenced by the work of Vaishnav and Pedram [15], Su *et al.* [16] and Kojima *et al.* [17] at the RT (architecture) level. As described earlier, the switching activity - wire length relation consists of three regions. Region A is characterized by $0 \leq l \leq l_1$. Switching activity in this region is given by

$$\omega_l = \Omega_1 \alpha^{-\frac{l}{l_1}} \quad (1)$$

where

$$\begin{aligned}\Omega_1 &= \text{switching activity on short wires (in transitions per clock period),} \\ \bar{l} &= \text{average wire length,} \\ l_1 &= \frac{1}{2} \bar{l}, \text{ and} \\ \alpha &\text{ is a constant } > 0.\end{aligned}$$

In region B , characterized by $l_1 < l \leq l_2$, the switching activity is constant, denoted Ω_m ; where $l_2 = \frac{3}{2} \bar{l}$. Region C is characterized by $l_2 < l \leq l_{max}$. In this region, the switching activity is given by

$$\omega_l = \Omega_2 \beta^{\frac{l-l_{max}}{\bar{l}}} \quad (2)$$

where

$$\begin{aligned}\Omega_2 &= \text{Switching activity on very long wires,} \\ l_{max} &= \frac{5}{2} \bar{l}, \text{ and} \\ \beta &\text{ is a constant } > 0.\end{aligned}$$

From Eq. (1) and Eq. (2), α and β are computed as

$$\ln \alpha = 2 \ln \frac{\Omega_1}{\Omega_m} \quad (3)$$

$$\ln \beta = \ln \frac{\Omega_2}{\Omega_m} \quad (4)$$

At this point we do not know the impact of this coarse model of switching activity on power prediction accuracy. However, a more elaborate model could be used and the overall method for power prediction would still be valid.

4.1.3 Mathematical model to predict functional unit power

A task implemented by a chip consists of one or more types of functions such as addition and multiplication. Let functional unit \mathcal{F}_j , used to implement function j consist of \mathcal{S}_j standard cells and \mathcal{N}_j nets. The average length of a wire in this unit, given by Feuer's formula [18] is

$$\bar{l}_j = \sqrt{2} \frac{2r_m(3+2r_m)}{(1+2r_m)(2+2r_m)} \frac{\mathcal{S}_j^{r_m-\frac{1}{2}}}{(1+\mathcal{S}_j^{r_m-1})} \times \bar{l}_\sigma \quad (5)$$

r_m is the Rent's exponent for macro cells or functional units. Kurdahi and Liu et al. reported in [8, 11] that r_m approximately equals 0.7. \bar{l}_σ is the average standard cell length. Consider an event where the length of a randomly selected wire/net in this unit equals l . Kurdahi showed that the probability density function for this event is geometric and that the parameter of the function is the reciprocal of the average length. Thus, the total number of nets in \mathcal{F}_j of length l is given by

$$N_j^l = \left(\frac{1}{\bar{l}_j}\right) \left(1 - \frac{1}{\bar{l}_j}\right)^{l-1} \times \mathcal{N}_j \quad (6)$$

The average switching capacitance associated with a net of length l in \mathcal{F}_j is given by

$$C_j^l = \mu \cdot l + C_\sigma \quad (7)$$

where

- μ = Capacitance of the metal wires (including contacts) per unit length, and
- C_σ = Average switching capacitance associated with a standard cell.

The average switching capacitance associated with a standard cell comprises the average input capacitance, the average output capacitance and the average internal capacitance of the standard cell.

As described earlier, switching activity on the nets is assumed to be a function of the net length. Total energy per cycle consumed by a functional unit \mathcal{F}_j during one isolated use is obtained by combining Equations (1), (2), (6) and (7).

$$E_{\mathcal{F}_j} = \frac{1}{2} \text{Vdd}^2 \cdot \left[\sum_0^{l_1} C_j^l \cdot N_j^l \cdot \Omega_1 \alpha^{-\frac{l}{\bar{l}_j}} + \sum_{l_1}^{l_2} C_j^l \cdot N_j^l \cdot \Omega_m + \sum_{l_2}^{l_{max}} C_j^l \cdot N_j^l \cdot \Omega_2 \beta^{\frac{l-l_{max}}{\bar{l}_j}} \right] \times d_j \quad (8)$$

where

- l_1 = $\frac{1}{2} \bar{l}_j$
- l_2 = $\frac{3}{2} \bar{l}_j$
- l_{max} = $\frac{5}{2} \bar{l}_j$ and
- d_j = Delay of \mathcal{F}_j (in ns.)

Abstractly, the model computes average power consumption in a functional unit as a function of unit length, switching activity, number of wires, and delay of the functional unit.

4.2 Estimating power consumption for a design

4.2.1 Functional units

For a function type j , the number of functional units (or operators) required by design i is estimated by BEST [10]:

$$\begin{aligned} O_j^i &= \left\lceil \frac{n_j^e \times \lceil \frac{d_j}{c} \rceil}{T^i} \right\rceil && \text{for the non-pipelined case} \\ &= \left\lceil \frac{n_j^e \times \lceil \frac{d_j}{c} \rceil}{L^i} \right\rceil && \text{for the pipelined case} \end{aligned} \quad (9)$$

where

- n_j^e = the effective number of operations of type j ,
- d_j = the delay of the operator,
- c = the clock period,
- T^i = the number of steps taken to complete the task by design i and,
- L^i = the initiation rate for design i (pipelined designs only).

Consider R repeated executions of the given task. The average utilization factor of the operators \mathcal{F}_j in design i is

$$\begin{aligned} U_j^i &= \frac{n_j^e \times \lceil \frac{d_j}{c} \rceil}{O_j^i \times T^i} && \text{for the non-pipelined case} \\ &= \frac{n_j^e \times \lceil \frac{d_j}{c} \rceil \times R}{O_j^i \times ((R-1)L^i + T^i)} && \text{for the pipelined case} \end{aligned} \quad (10)$$

where utilization is the percentage of time a functional unit is being used. From Equations (8), (9) and (10) the expression for the average power consumed by *all* functional units in a design i is written as

$$P_{\mathcal{F}}^i = \frac{\sum_j O_j^i \times U_j^i \times E_{\mathcal{F}_j}}{c} \quad (11)$$

4.2.2 External nets

Let the total number of external nets (nets extending outside a functional unit) for design i given by BEST be \mathcal{N}^i . The average length of external wires in this design given by Feuer's formula is

$$\bar{l}^i = \sqrt{2} \frac{2r_c(3 + 2r_c)}{(1 + 2r_c)(2 + 2r_c)} \frac{O^{i r_c - \frac{1}{2}}}{(1 + O^{i r_c - 1})} \times \bar{l}_{\mathcal{F}^i} \quad (12)$$

where

- r_c = Rent's exponent for chips (its value approximately equals 1.0).
 $\mathcal{O}^i = \sum_j \mathcal{O}_j^i$, is the number of operators in design i
 $\bar{l}_{\mathcal{F}^i} = \frac{\sum_j \mathcal{O}_j^i \cdot (\mathcal{H}_j + \mathcal{W}_j)}{2\mathcal{O}^i}$, is the average length of functional units in design i
 \mathcal{H}_j = Height of operators \mathcal{F}_j and
 \mathcal{W}_j = Width of operators \mathcal{F}_j

Once again, using the geometric distribution, the total number of nets in design i of length l is

$$N^{li} = \left(\frac{1}{\bar{l}^i}\right) \left(1 - \frac{1}{\bar{l}^i}\right)^{l-1} \times \mathcal{N}^i \quad (13)$$

and, the average switching capacitance associated with a net of length l in the chip is

$$C^{li} = \mu \cdot l + C_\sigma \quad (14)$$

Net length - switching activity assumptions made in Section 4.1.2 also hold at the chip level. Functional units exchanging data frequently are more likely to be placed in close proximity. In addition, very long wires carrying global control signals and clock have higher switching probabilities. Thus, the average power consumed by the switching activity on the external nets is given by

$$P_{\mathcal{N}}^i = \frac{\frac{1}{2} V_{dd}^2 \cdot \left[\sum_0^{l_1} C^{li} \cdot N^{li} \cdot \Omega_1 \alpha^{-\frac{l}{\bar{l}^i}} + \sum_{l_1}^{l_2} C^{li} \cdot N^{li} \cdot \Omega_m + \sum_{l_2}^{l_{max}} C^{li} \cdot N^{li} \cdot \Omega_2 \beta^{\frac{l-l_{max}}{\bar{l}^i}} \right]}{c}} \quad (15)$$

where

$$\begin{aligned}
 l_1 &= \frac{1}{2} \bar{l}^i \\
 l_2 &= \frac{3}{2} \bar{l}^i, \text{ and} \\
 l_{max} &= \frac{5}{2} \bar{l}^i
 \end{aligned}$$

Finally, the average chip power for design i is the sum of the total average functional power and average external net power given by Equations (11) and (15):

$$P_{chip}^i = P_{\mathcal{F}}^i + P_{\mathcal{N}}^i \quad (16)$$

Abstractly stated, the average chip power can be predicted based only on the behavioral description, a simplified model of switching activity, information about total size and delay of predicted functional units, the clock period used in the design, predicted capacitance of the interconnect used in the design, and layout characteristics of the design style.

4.3 The energy/power prediction algorithm

PREDICTPOWER

Use BEST to generate all prediction points

For each prediction point

/ External interconnect energy */*

Compute average width/length of functional operators

/ Their counts are given by BEST and dimensions by PROMAN² */*

Use Feuer's formula to compute the average external wire-length.

Use geometric distribution and wire-length, switching activity correlation to compute the external net energy consumption.

/ Total number of external nets is given by BEST */*

/ Functional unit energy */*

For each functional unit

Use the number of constituent standard cells and the number of nets obtained from PROMAN.

Compute the average wire-length using the average standard cell width.

Use geometric distribution and wire-length, switching activity correlation and the average standard cell switching capacitance to compute the internal net energy consumption.

Accumulate the internal net energy consumption.

Total energy \leftarrow external net energy + accumulated internal net energy.

Average power \leftarrow total energy / delay of the predicted design

5 Experimental verification

Energy and power consumption estimates were generated for the design space of two data-flow graphs, namely, AR-FILTER and 1-D DCT (discrete cosine transform). Three designs for AR-FILTER and two

² Layout analysis tool in the CASCADE Design Automation's suite of tools for physical design

designs for DCT were selected, each with different execution delay. These designs were then synthesized to obtain RT-level net-lists using the USC suite of tools [19]. Physical designs were generated for these net-lists using CASCADE Design Automation's tools EPOCH and PROMAN. A few commonly used macro cells such as Booth's multiplier, look-ahead and ripple-carry adders, and registers were pre-synthesized to be used in the synthesis of these data paths. Finally, power estimates for the synthesized designs were obtained from PROMAN. Although our predictor is well suited for many design styles, we chose standard cell design for the purpose of our experiments and the layout process used was MOSIS 1.2 μm . double-metal single-poly. Library information on standard cells and macro cells required by the power predictor is listed in Tables 1 and 2. Comparison results are shown in Table 3.

Table 1: Standard cell data

i	# gates	53
ii	# inputs	206
iii	Average width	42 μm
iv	Average internal capacitance	34 fF
v	Average gate input capacitance	225 fF
vi	Average output capacitance	30 fF
vii	Average total switching capacitance	100 fF
viii	Average transistor-gate pair capacitance	58 fF
ix	Metal and Via capacitance	0.22 fF/ μm

The 1-D DCT example is fairly large and has over 400 nodes. Notice, that the design that requires 20 steps consumes significantly more energy than the one requiring 8 steps. Average power consumption in either case is comparable because additional functional operators in the faster design are replaced by

Table 2: Macro cell data

Name	# standard cells	# 2-point nets	Dimensions ($\mu\text{m} \times \mu\text{m}$)	Delay (ns)
16-bit adder	48	97	811x231	15
16-bit subtracter	64	113	88x874	15
16-bit multiplier	1320	1225	991x1181	85
16-bit register	80	83	676x82	2
16-bit multiplexer	32	67	650x56	2

Table 3: Experimental results

Design	Delay (steps)	Predicted function energy (μJ)	Predicted external net energy (μJ)	Predicted total energy (μJ)	Predicted power (mW)	PROMAN power (mW)
AR-FILTER	7	21.00	30.90	51.90	74.10	71.51
AR-FILTER	9	18.20	39.80	58.00	64.40	59.46
AR-FILTER	18	17.70	75.90	93.60	52.30	49.02
DCT	8	37.00	110	147	229	213
DCT	20	44.70	279	323.70	202	202

several multiplexers and nets in the slower one. Figure 4 shows how the estimates of function, interconnect, total energy and average power vary with the execution delay for the DCT example.

6 Conclusions

We have presented a comprehensive system-level energy/power predictor that explores the vast design space prior to requiring the designer to make critical design choices. Results obtained are accurate yet the predictor is fast (In the 1-D DCT example, 72 designs were analyzed in 600 milliseconds). This is achieved mainly due to statistical modeling of the target chip and its building blocks or functional

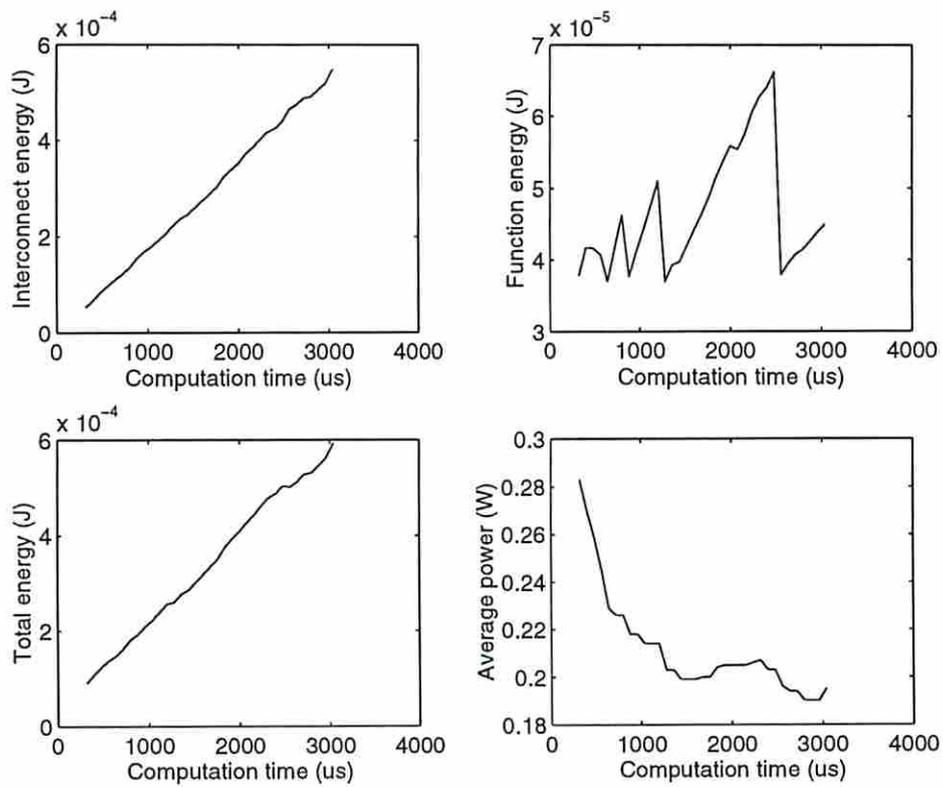


Figure 4: Variation in estimated DCT energy/power consumption with delay

operators as a group of switching nets. The estimator can be used to predict power for both pipelined and non-pipelined implementations of algorithms. In either style, there are highly parallel and highly sequential designs and the energy/power characteristic of each one is predicted. Thus, during the synthesis steps, the designer is now able to control the search space more efficiently such that circuits with desired cost, performance, battery life and thermal characteristics are synthesized. Results obtained from our predictor could also be used to partition a single task over one or more chips. Although we have assumed the standard cell layout style in our experimental verification (albeit in a loose way, since EPOCH layouts are not strictly standard cell style), it is possible to extend our work to gate array and FPGA layout styles. Furthermore, our predictor can be readily used with different technologies by simply changing the technology parameters embedded in BEST and in our power predictor.

7 Acknowledgments

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